LVR Feature Datasheet

Design Rule Layout Verification Suite

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LVR delivers high-performance physical verification for modern IC designs. With production-proven DRC and LVS engines, it scales efficiently to handle designs with tens of millions of devices, ensuring reliable signoff at advanced technology nodes.

Benefits

Proven Accuracy at Scale
Trusted by industry leaders, the tool delivers production-grade accuracy for rule checking and netlist verification across complex, high-density designs.

Unified Signoff Platform
A comprehensive, single-vendor solution covering implementation through DRC/LVS/ERC signoff, eliminating the fragmentation of using multiple tools.

Effortless Debug and Root Cause Analysis
Visual and scriptable debug environments with layout and netlist cross-probing significantly reduce time spent resolving violations.

Seamless Format Compatibility
Built-in support for industry-standard formats like GDS, CDL, and Verilog ensures hassle-free adoption and migration.

Scalable Compute, Lower Cost
Leverages multithreaded and distributed computing across standard compute farms, delivering high performance without additional hardware investment.

Key Features

DRC (Design Rule Check)
Comprehensive rule-based geometric verification engine that checks all physical design constraints—such as spacing, width, enclosure, extension, and minimum/maximum rules. Scales efficiently for advanced nodes with hierarchy-aware rule processing.

LVS (Layout vs Schematic)
Performs structural and connectivity-level netlist comparison between layout and schematic. Identifies shorts, opens, missing or extra devices, and mismatched pins. Includes support for black-box macros, parameterized devices, and netlist format translations.

ERC (Electrical Rule Check)
Detects electrical violations such as unconnected pins, floating gates, missing power/ground, and conflicting drive strengths. Performs context-aware evaluation across hierarchical blocks.

SVS (Schematic vs Schematic)
Compares two schematic netlists to ensure functional equivalence, typically used for golden vs revised schematics or post-ECO comparisons. Supports logical net renaming and black-box instance matching.

Density Check
Analyzes metal density across configurable windows to ensure uniform planarization and etch consistency. Flag low/high density regions and suggest fill recommendations.

XOR (Fast XOR Comparison)
Efficient binary geometric diff engine that highlights any divergence between two layouts. Useful for ECO validation, revision control, and sign-off release verification. Supports marker generation and rule-tolerant matching.

Advanced Capabilities

Multithreaded Processing
Designed with a thread-parallel architecture that utilizes all available CPU cores to accelerate rule evaluation and geometric computation. Each rule or chip region is intelligently partitioned for optimal concurrency.

TCL Scripting Support
Complete TCL interpreter embedded for rule customization, batch scripting, flow automation, and parameter tuning. All rule decks and reports are TCL-extensible.

Extensive Documentation
Over 3000 pages of fully indexed user guides, developer references, and integration manuals—covering DRC, LVS, scripting, file formats, and debug workflows.

Application Notes
Includes a library of 50+ application notes covering real-world design problems, debugging cases, optimization tips, and best practices across technology nodes.

24x7 Support
Dedicated support engineers available globally to resolve issues with fast turnaround, including live debugging sessions, remote collaboration, and critical path triage.

GUI Debug Environment
Integrated visual interface with GDS viewer, netlist browser, and interactive rule debugger. Supports cross-probing and overlay of error markers directly on layout or schematic.

Violation Histograms

Generates statistical plots to analyze frequency, distribution, and severity of violations—helping designers identify hotspots, optimize rule coverage, and prioritize fixes.

Detailed Error Reports

Generates comprehensive and hierarchical violation reports, grouped by rule, instance, or region. Includes hyperlinks to layout and suggestions for correction.

Marker Browser

All features are backed by a marker engine that generates GDS markers and overlays to assist in pinpointing exact problem locations. Integrated into GUI for instant feedback.

Technical Specifications

- **Supported Operating Systems:** Ubuntu 22.04, RedHat 9.5, macOS Monterey
- **Max Design Size:** 100 million gates
- **License Model:** Per-core floating license
- **Supported Formats:** GDS, Verilog, CDL

Contact Us

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