Ramtera & LVR Overview

Layout Verification & Reporting Suite

Ramtera Design Automation

December 2025

Ramtera at a Glance

- **Company:** Ramtera Design Automation (EDA software)
- **Registered Office:** Delaware USA
- **Flagship:** LVR Layout Verification & Reporting suite
- **Focus:** DRC, LVS, ERC, Density, XOR, GUI, Docs, TCL support
- **Positioning:** High-performance, developer-friendly, scalable PV toolchain
- **Platforms:** Ubuntu, Red Hat, macOS (standalone binary)

Problem & Opportunity

- **Pain today:** Long PV runtimes, complex rule decks, heavy debug cycles
- **Gaps:** Usability, openness for customization, cost at mature nodes
- **Opportunity:** A modern, fast, transparent PV suite for digital/AMS teams
- **Ramtera Edge:** Lean footprint, strong docs, rapid iteration, customer-centric features

LVR Overview

- **What it is:** A production-ready PV suite for *DRC/LVS/ERC/Density/XOR* with Debug GUI
- **Design Scale:** Up to 1T devices (current target)
- **Rule Decks:** SVRF-like LRF; TCL scripting; comprehensive reporting
- **Deliverables:** Executables, sample designs, rule packs, docs, support

Architecture & Tech Stack

- **Core:** C++ (Boost Polygon), multi-threaded execution
- **Geometry:** Polygon90/Polygon90Set with R-tree acceleration
- **I/O:** GDS/DEF/LEF, SPICE/Verilog conversions, GDS export
- **Scripting:** TCL integration, batch automation
- **GUI:** Qt-based debug views; markers, error browse, histograms

Key Modules

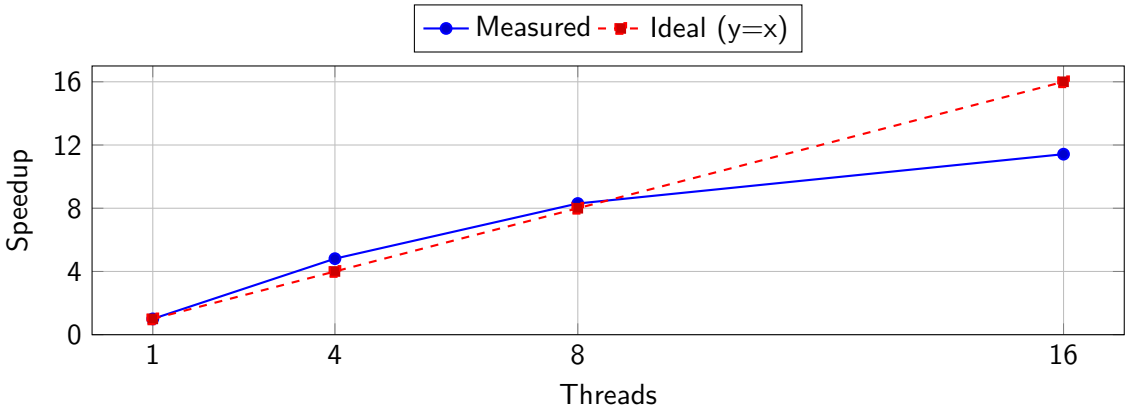
- **DRC:** Width/spacing, enclosure, density windows, fast-XOR, LEF/DEF checks
- **LVS:** Netlist extraction, std-cell matching, shorts/opens, schematic-vs-schematic
- **ERC:** Power/ground checks, multiple drivers, pin connectivity
- **Density:** Window-based analysis, summaries, markers
- **XOR:** Revision/stream-to-stream diffs for signoff audits
- **GUI:** Debug, Browse Markers, Report views, Histograms

Performance & Benchmarks

- **Multicore Scaling:** Internal tests show 10+ x speedups on multicore runs
- **Distributed Computing:** Internal DRC tests show 1 to 12 minutes for 100M polygons
- **Examples:** Up to $\tilde{1}1.4\times$ on 16 cores (design-dependent)
- **Footprint:** Lean memory, fast load; designed for mature-node throughput
- **Road to 32c:** Active work on scaling

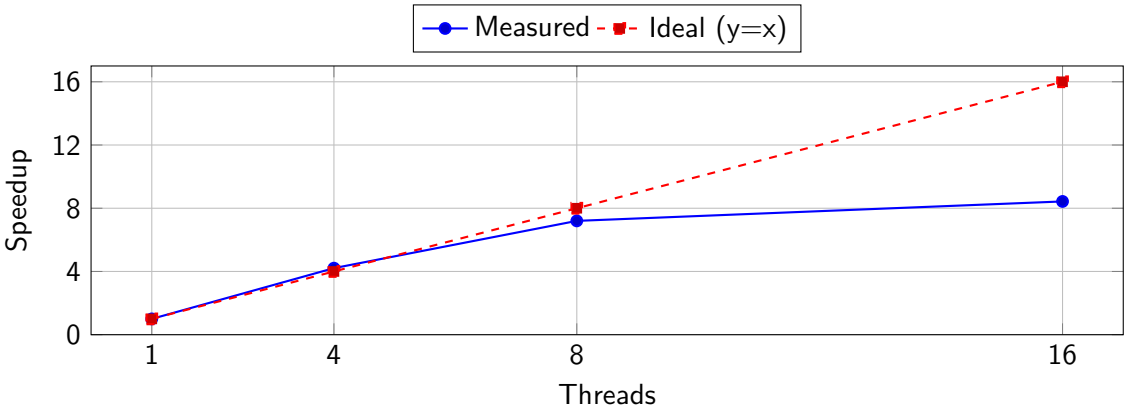
sky130 | DRC | jpeg_encoder1

Peak: 16c → 11.42× (71.4%)



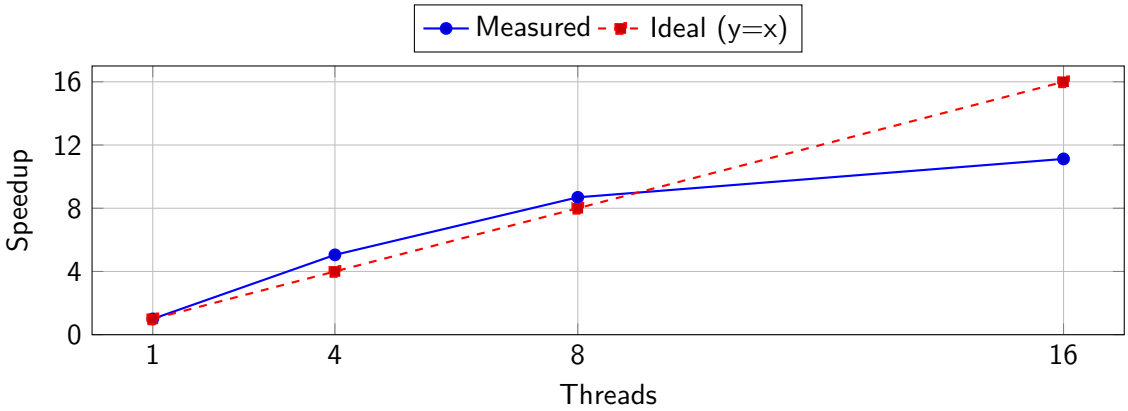
sky130 | DRC | jpeg_encoder2

Peak: 16c → 8.43× (52.7%)



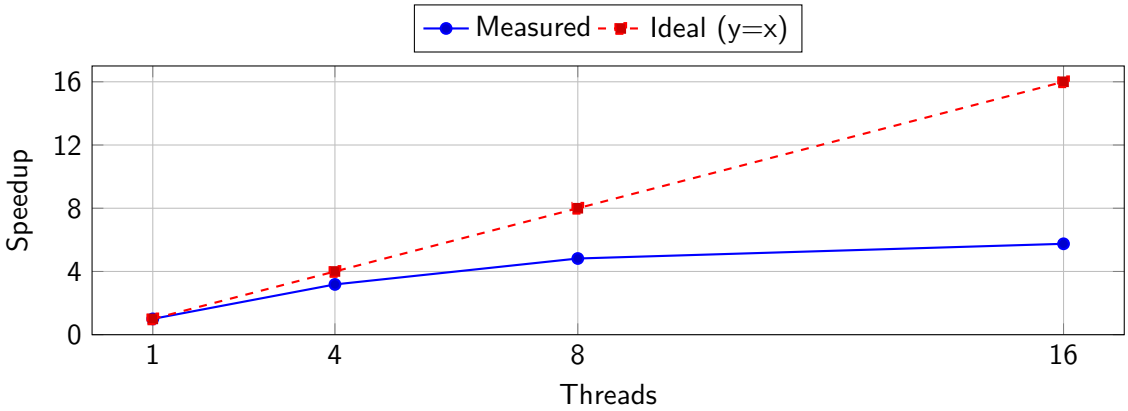
sky130 | DRC | jpeg_encoder3

Peak: 16c → 11.12× (69.5%)



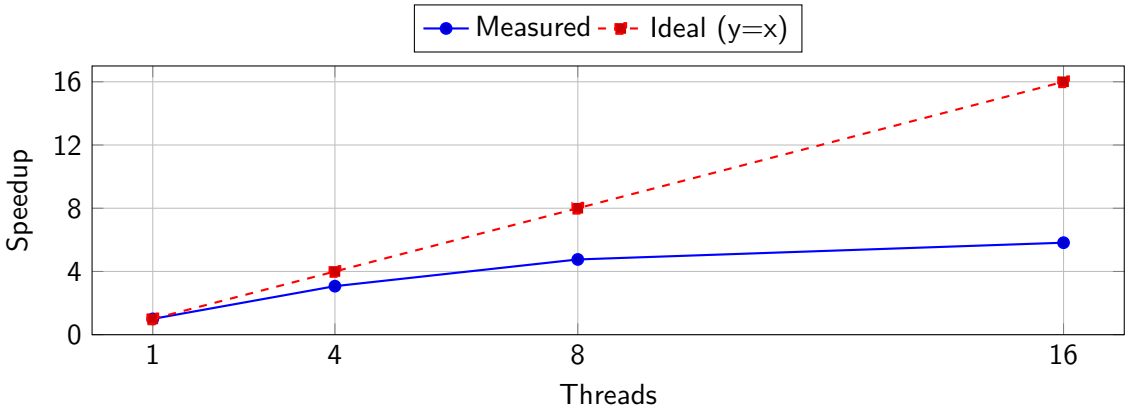
sky130 | ERC | jpeg_encoder1

Peak: 16c → 5.75× (35.9%)



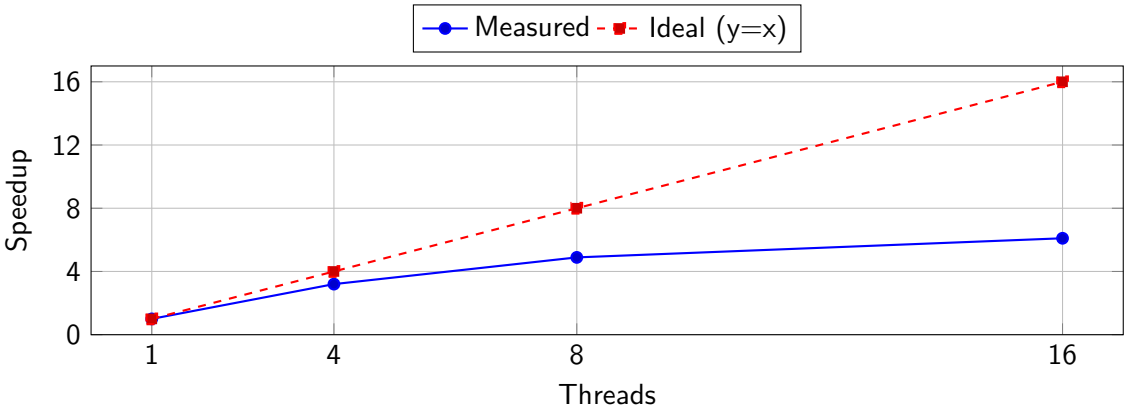
sky130 | ERC | jpeg_encoder2

Peak: 16c → 5.82× (36.4%)



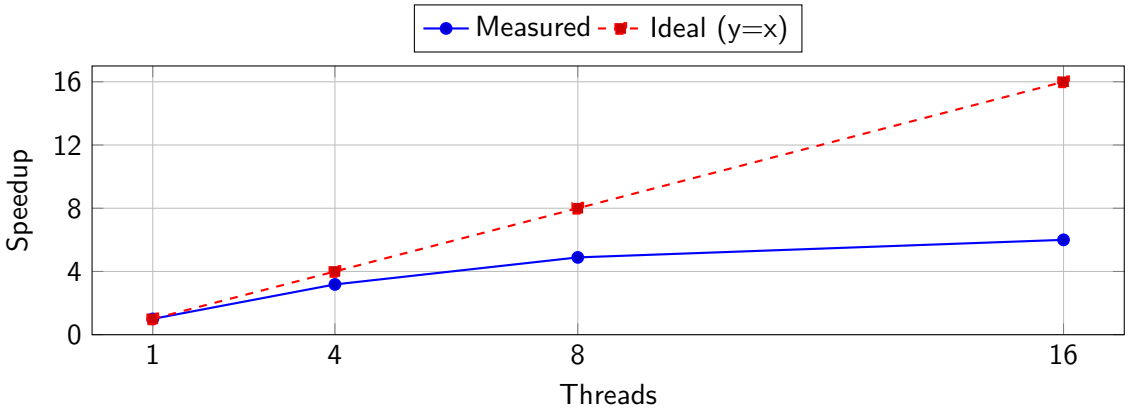
sky130 | ERC | jpeg_encoder3

Peak: 16c → 6.10× (38.1%)



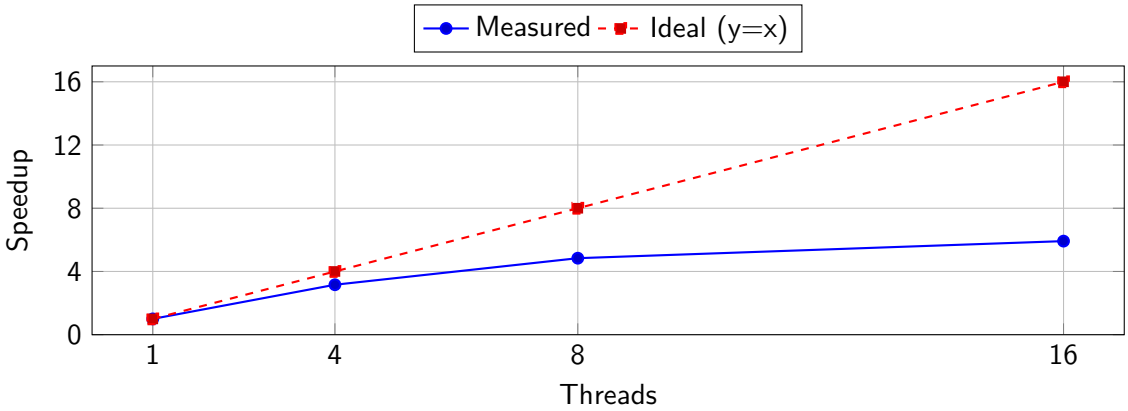
sky130 | LVS | jpeg_encoder1

Peak: 16c → 6.00× (37.5%)



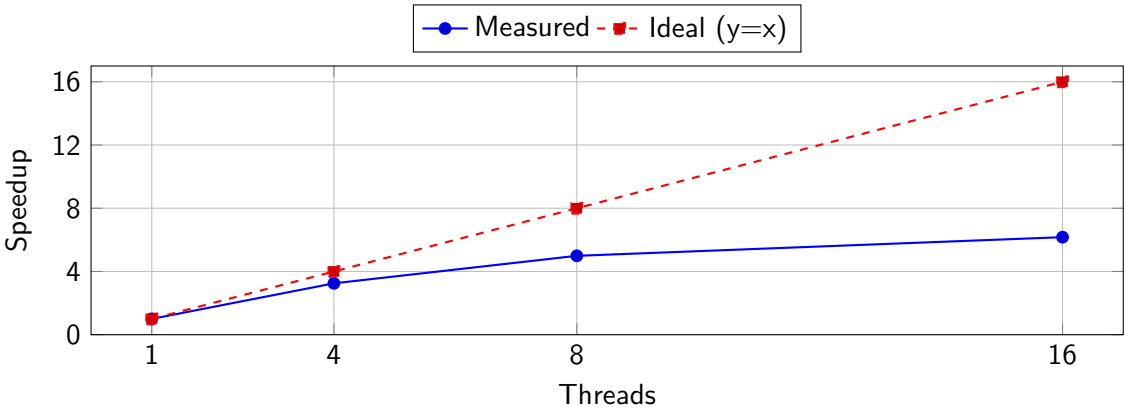
sky130 | LVS | jpeg_encoder2

Peak: 16c → 5.92× (37.0%)



sky130 | LVS | jpeg_encoder3

Peak: 16c → 6.17× (38.6%)



Proven Tech Nodes & Validation

- **LVS Proven:** Sky130HD , Nangate45, SG13G2 (comprehensive rule implementation)
- **DRC Proven:** Sky130HD, Nangate45 , SG13G2 (robust rule support including density, XOR)
- **Validation:** Regression suite with open-source designs; logs and reports
- **Target Support:** Focused set of nodes with expanding coverage

IP, Docs & Compliance

- **Patents:** Multiple filings in US & India (*patent pending*)
- **Docs:** 1,000+ pages tutorials, user guide, error catalogs, examples, results
- **Compliance:** Clean-room engineering; respect for foundry/PDK NDAs
- **Licensing:** Node-agnostic architecture; per-seat annual licensing

GUI layout viewer

Figure: Screenshot of LVR Viewer/Debugger

Histograms

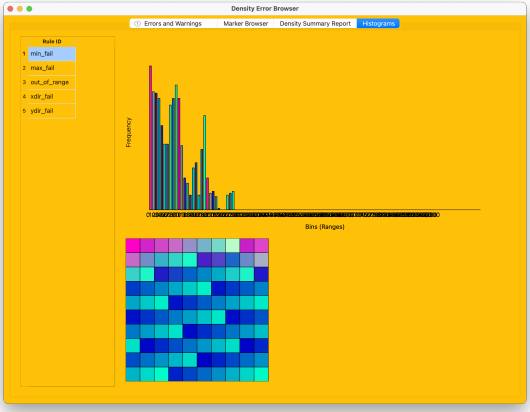


Figure: Screenshot of LVR Density Histogram

Error Report Browsers

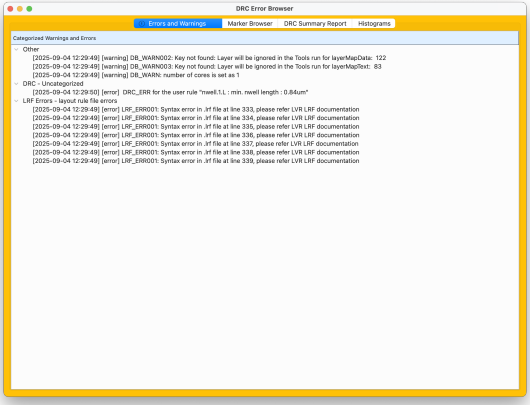


Figure: Screenshot of LVR Error Report Browser

Summary Report Browsers

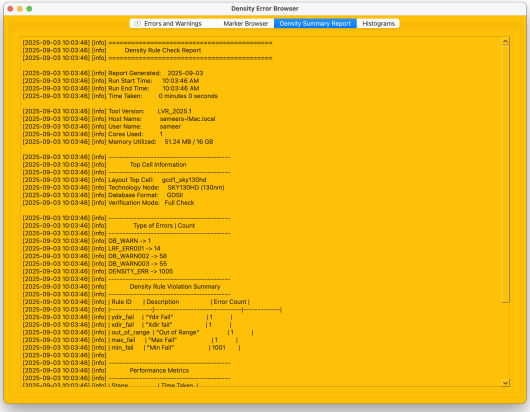


Figure: Screenshot of LVR Summary Report Browser

Pricing & Licensing

LVR Standard

- DRC, LVS, ERC, XOR, Density
- Debug GUI, TCL, Docs
- Up to 1T devices
- Multi-OS executables

Advanced / Enterprise

- Advanced: DFM, Antenna, MT optimizations, custom rules
- Enterprise: PERC, priority support, certifications
- Volume discounts, multi-year options

Pricing available on request; tailored to deployment size and support level.

Roadmap (Next 36 Months)

- Scale Distributed Multicore performance and memory optimizations for 1T polygons
- Expand rule coverage on focus nodes; add regression breadth
- Strengthen GUI flows (debug markers, ECO ops, usability polish)
- Documentation: API refs, cookbook examples, best-practice guides
- Optional: DFM/Antenna features subject to demand

Patents, Copyrights and Trademarks, Partnerships

- 4 USPTO Patents that achieve 10x speedup, complex parsing capabilities
- 5 Indian Patents that achieve highly scalable Distributed computing
- Offices maintained in New York, Delaware, Bangalore
- 5 Copyrights, 4 Trademarks
- Qualified Partner with Intel, Google, Broadcom, Amazon
- Invited Talks ICEE IEEE
- Exhibit Booths ICEE (Bangalore) VLSID (Pune) Chiplet Summit (Santa Clara) DAC (Long Beach)
- Record benchmark of 1 trillion polygon DRC in 11 hours

Contact & Call to Action

- **Website:** https://www.ramtera.com
- **Email:** sameer@ramtera.com
- **What we offer:** Fast evaluation, hands-on demos, and collaborative pilots
- **Ask:** Explore a pilot or strategic partnership to accelerate your PV flow

Thank you!