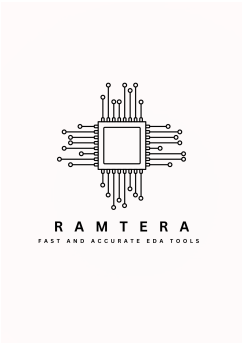

LVR: Layout Verification Reporter

Powering Accurate DRC and LVS for Modern IC Designs

Key Features

- Advanced DRC (Design Rule Check)
- High-Speed LVS (Layout Versus Schematic)
- Multithreaded and Multi CPU usage
- Support for Industry Rule decks
- Multi-Node Technology Support
- Multi-million Gate Support

Why Choose LVR?

- Improved Accuracy with Cutting-Edge Algorithms
- Easy Integration with Existing EDA Flows
- Supports Industry standard GDSII and LEF DEF formats
- Comprehensive Reporting and Analysis
- Reduced Time-to-Market and custom

Performance

Efficiency: Up to 3x faster checks compared to leading tools.
Scalability: Handles large designs seamlessly.

Use Cases

IC Manufacturing: Ensures compliance with DFM rules.
EDA Companies: Seamlessly integrates into workflows.

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Fast and Accurate EDA tools