	In Progress
	Completed
	Heading

DRC	LVS	DFM	GUI	ERC	TECH NODES
Width Rule Check	Device Extraction	DFM_PROPERTY: Width Annotation Test	Marker Browser	Power Shorts	sky130hd
Spacing Rule Check	Netlist Extraction	DFM_FILL: Dummy Fill Insertion Test	Error Report Browser	Ground Shorts	sky130hs
Enclosure / Overlap	Analog designs	VIA Redundancy Detection Test	Summary Browser	Unconnected Ports	ng45
Minimum Area Checking	Netlist Matching	DFM_SLOTTING Test	Marker Screen Navigation		ng15
OffGrid, Rect_Only, Width_Table	Shorts	DFM_SERPENTINE Test	Instance Search dialog	**Density**	saed32
Via / Cut Spacing Check	Open	DFM_HOTSPOT Pattern Match Test	Net Search Dialog	Min Density	gpdk90
Pattern-Matching Rules	Tested on 4 Nodes	Critical Area Analysis (CAA) Test	Graphics Viewer	Max Density	sg13g2
Multi-Patterning Verification		Litho-Friendly Design Check	Layer Control Panel	Density Range	saed14
DRC Waiver Flow	**SVS**	CMP Analysis Test	SelectionPanel		gf180
Debug Environment	Schematic V/S Sche	Edge Proximity Filter Test		**XOR**	asap7
Testing on 10 Nodes in progress	Verilog V/S verilog	1.6 billion polygons in 1 minute		Layout V/S Layout	xh018
Fast Distributed Computing		Fast Distributed Computing		comparison	
1 Trillion polygon in 11 hours					
1.6 billion polygons in 1 minute					