LVR Layout Rules Format (LRF) User Guide

Ramtera Inc

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LVR
Layout Verification
Reporter

Contents

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1 LRF (Layout Rules File Reference

1.1 `size (extent) -by 1.0 -layerOut bulk`

Description.

The `size` command reshapes geometry by performing an offset (grow or shrink) operation. In `extent` mode, it operates on the bounding extent of the input layer rather than on each polygon independently. Conceptually, the engine computes the minimal axis-aligned bounding rectangle that covers all shapes in the source layer and then expands or contracts that rectangle by the value supplied after `-by`.

This is useful for constructing guard or keep-out regions, enlarging search regions before subsequent Boolean operations, and creating context envelopes for checks such as enclosure or minimum surround. Because the operation is applied to a global extent rather than to each polygon, it preserves the overall footprint while smoothing small interior details.

Implementation notes: offsetting is usually Manhattan (L_1 metric) in sign-off decks to ensure deterministic grid snapping. Very large positive values of `-by` can cause the extent to overlap regions that were previously separated, which is sometimes intentional (e.g., to force a unified analysis box). Negative values contract the extent and may clip valid shapes—this is occasionally used to test margins under worst-case misalignment assumptions.

Edge cases to consider include empty inputs (which should yield an empty result), degenerate single-point extents, and numerical robustness near the database unit. The output can be emitted to a named layer via `-layerOut`; when omitted, the sized extent remains in the evaluation pipeline for subsequent operations.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`size`	keyword	yes	—	Operation name.
`(extent)`	enum	yes	—	Operate on global bounding extent.
`-by <float_value>`	flag+number	yes	—	Offset amount; positive=grow, negative=shrink.
`-layerOut <output_layer>`	flag+layer	optional	—	Destination for the resulting extent.

Example Usage.

```
size (extent) -by <float\_value> -layerOut <output\_layer>
```

1.2 `not bulk NWELL -layerOut PWELL`

Description.

The `not` operator performs Boolean subtraction: all shapes from the first operand that overlap the second operand are removed. Here, subtracting `NWELL` from `bulk` yields the complement region (commonly called `PWELL` in technologies where the substrate is p-type). This derived region is used to drive checks that target features located outside wells, such as taps or implants that must reside strictly in the substrate.

Algorithmically, subtraction is computed per polygon with robust polygon clipping. The engine preserves layer semantics (datatypes, hierarchy) according to tool policy; most decks flatten for Boolean evaluation to avoid aliasing at cell boundaries. If `-layerOut` is specified, the result is materialized on the given layer, enabling reuse in subsequent rules and clear visualization in debug. When `NWELL` overlaps `bulk` exactly at an edge (touching but not overlapping), the treatment is implementation-defined; sign-off decks typically treat touching edges as non-overlap to avoid spurious slivers.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`not`	keyword	yes	—	Boolean subtraction A.
`bulk`	layer	yes	—	Minuend (A).
`NWELL`	layer	yes	—	Subtrahend (B).
`-layerOut PWELL`	flag+layer	yes	—	Output layer for A.

Example Usage.

```
not <layer1\_name> <layer2\_name> -layerOut <output\_layer>
```

1.3 `not bulk NWELL`

Description.

This form performs the same Boolean subtraction as the previous rule but keeps the result transient (piped to the next operation) rather than materializing it on a named layer. Use this when the result is an intermediate in a larger Boolean expression and does not need to be visualized or re-referenced.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`not`	keyword	yes	—	Boolean subtraction A.
`bulk`	layer	yes	—	Minuend (A).
`NWELL`	layer	yes	—	Subtrahend (B).

Example Usage.

```
not <layer1\_name> <layer2\_name>
```

1.4 `and DIFF NSDM -layerOut NDIFF`

Description.

The `and` operator computes the geometric intersection of two layers. Intersecting `DIFF` (active diffusion) with `NSDM` (n-type source/drain implant mask) produces n-diffusion (`NDIFF`). This is a canonical derivation used to classify device regions and to drive transistor recognition or implant-specific rules.

Intersection is robust to hierarchy and handles coincident edges. If either operand is empty, the result is empty. Persisting the result with `-layerOut` is useful for repeated reuse (e.g., contacts over NDIFF, enclosure checks, and antenna accounting).

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`and`	keyword	yes	—	Boolean intersection A ∩ B.
`DIFF`	layer	yes	—	Diffusion (active).
`NSDM`	layer	yes	—	N+ implant mask.
`-layerOut NDIFF`	flag+layer	yes	—	Output n-diffusion layer.

Example Usage.

```
and <layer1\_name> <layer2\_name> -layerOut <output\_layer>
```

1.5 `and DIFF NSDM`

Description.

Same intersection as above but transients the result in the evaluation pipeline. Use this form inside chained Boolean expressions to minimize the number of temporary layers while retaining clarity of intent.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`and`	keyword	yes	—	Boolean intersection.
`DIFF`	layer	yes	—	First operand.
`NSDM`	layer	yes	—	Second operand.

Example Usage.

```
and <layer1\_name> <layer2\_name>
```

1.6 `or PSD NSD -layerOut MYDIFF`

Description.

The `or` operator forms the geometric union of two layers. Combining `PSD` (p-type S/D implant) and `NSD` (n-type S/D implant) yields a generalized S/D implant region that can be convenient when rules apply to either polarity. Materializing the union with `-layerOut` enables downstream reuse for contact density, spacing-to-metal, or keep-out analyses.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`or`	keyword	yes	—	Boolean union A ∪ B.
`PSD`	layer	yes	—	P+ implant mask.
`NSD`	layer	yes	—	N+ implant mask.
`-layerOut MYDIFF`	flag+layer	yes	—	Output union layer.

Example Usage.

```
or <layer1\_name> <layer2\_name> -layerOut <output\_layer>
```

1.7 `or PSD NSD`

Description.

Same union as above, but the result remains in-flight for immediate consumption by subsequent operations. Use this for concise one-liners that derive generalized regions without cluttering the namespace with temporary layers.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`or`	keyword	yes	—	Boolean union.
`PSD`	layer	yes	—	First operand.
`NSD`	layer	yes	—	Second operand.

Example Usage.

```
or <layer1\_name> <layer2\_name>
```

1.8 get_corners DIFF -layerOut CD

Description.

get_corners extracts polygon corner features from the input layer. Corners are typically identified by evaluating interior angles at vertices; for orthogonal layouts, corners are usually 90° or 270°, but corner classification can include convex vs. concave, acute vs. obtuse, and minimum radius criteria.

This command is commonly used to detect notch-prone shapes, to drive corner smoothing rules, or to locate places where additional enclosure or spacing is required due to lithographic sensitivity. Emitting the result to an output layer (CD) allows visualization of the corner markers and correlation with downstream spacing or enclosure checks.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`get_corners`	keyword	yes	—	Corner feature extraction.
`DIFF`	layer	yes	—	Source layer.
`-layerOut CD`	flag+layer	yes	—	Output layer for corner markers.

Example Usage.

```
get\_corners <layer1\_name> -layerOut <output\_layer>
```

1.9 get_corners DIFF

Description.

Same as above without emitting an explicit output layer. Use when corner features are immediately filtered or combined with other feature-extraction commands.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_corners	keyword	yes	—	Corner extraction.
DIFF	layer	yes	—	Source layer.

Example Usage.

```
get\_corners <layer1\_name>
```

1.10 get_intersecting LICON DIFF -layerOut diff_licon

Description.

get_intersecting filters shapes from the first layer that geometrically intersect shapes from the second layer. Using LICON as the primary set and DIFF as the intersect-with set yields contacts placed over active diffusion. This derived subset is widely used to check enclosure of contacts by implant or well, to count contact density, or to compute antenna contributions.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_intersecting	keyword	yes	—	Retain shapes from A that intersect B.
LICON	layer	yes	—	Primary set (candidate shapes).
DIFF	layer	yes	—	Intersect-with set.
-layerOut diff_licon	flag+layer	yes	—	Output subset layer.

Example Usage.

```
get\_intersecting <layer1\_name> <layer2\_name> -layerOut <output\_layer>
```

1.11 get_intersecting LICON DIFF

Description.

Same intersection as above, but the result remains transient for subsequent processing. This is convenient when the intersected subset feeds immediately into spacing, enclosure, or sizing operations.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_intersecting	keyword	yes	—	Filter by intersection.
LICON	layer	yes	—	Primary set.
DIFF	layer	yes	—	Intersect-with set.

Example Usage.

```
get\_intersecting <layer1\_name> <layer2\_name>
```

1.12 enclosure -all_side VARAC NWELL -lt 0.15

Description.

enclosure measures how much a target layer surrounds a reference layer. The -all_side mode requires that the enclosing layer (here NWELL) meets the threshold on every side of the inner layer (VARAC). The comparator -lt flags locations where the measured enclosure is less than the specified margin.

Typical uses include ensuring that sensitive devices (e.g., varactors) sit within a protective region (well, guard ring) with adequate margin. Measurement can be implemented by dilating the inner layer by the required margin and checking that the result is completely contained within the outer layer, or by computing minimum edge-to-edge distances around the inner perimeter.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`enclosure`	keyword	yes	—	Measure surrounding margin.
`-all_side`	flag	yes	—	Require enclosure on every side.
`VARAC`	layer	yes	—	Inner (enclosed) layer.
`NWELL`	layer	yes	—	Outer (enclosing) layer.
`-lt <float_value>`	flag+number	yes	—	Flag if enclosure $<$ threshold.

Example Usage.

```
enclosure -all\_side <layer1\_name> <layer2\_name> -lt <float\_value>
```

1.13 `enclosure -all_side VARAC NWELL -lt 0.15 -layerOut temp`

Description.

Same as the previous rule but emits the failing (or measured) regions to a named layer for inspection. This is helpful to debug marginal margins around device edges and to attach error markers for reporting.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`enclosure`	keyword	yes	—	Measure surrounding margin.
`-all_side`	flag	yes	—	Require enclosure on every side.
`VARAC`	layer	yes	—	Inner (enclosed) layer.
`NWELL`	layer	yes	—	Outer (enclosing) layer.
`-lt <float_value>`	flag+number	yes	—	Flag if enclosure $<$ threshold.
`-layerOut <output_layer>`	flag+layer	yes	—	Materialize result.

Example Usage.

```
enclosure -all\_side <layer1\_name> <layer2\_name> -lt <float\_value> -layerOut <o
```

1.14 `enclosure -opposite_side licon_poly POLY -lt 0.08 -layerOut temp`

Description.

The `-opposite_side` mode measures enclosure on the side opposite a reference edge or anchor. This is useful when only one side of a feature needs a particular margin—for example, ensuring that a contact near the edge of a poly gate has adequate poly extension on the far side (opposite the contact edge). The `-lt` comparator flags insufficient enclosure relative to the threshold.

Internally, the tool identifies the reference side based on local edge normals or a designated anchor relationship between the two layers. Only the opposite side is evaluated; other sides may be below threshold without being reported by this rule.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`enclosure`	keyword	yes	—	Enclosure measurement.
`-opposite_side`	flag	yes	—	Measure on the opposite side only.
`licon_poly`	layer	yes	—	Inner or reference feature.
`POLY`	layer	yes	—	Enclosing/target layer.
`-lt <float_value>`	flag+number	yes	—	Flag if enclosure $<$ threshold.
`-layerOut <output_layer>`	flag+layer	yes	—	Emit result layer.

Example Usage.

```
enclosure -opposite\_side <layer1\_name> <layer2\_name> -lt <float\_value> -layerO
```

1.15 `enclosure -opposite_side licon_poly POLY -lt 0.08`

Description.

Same as the previous opposite-side enclosure check but leaves the result transient for immediate use in chained checks without materializing an output layer.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`enclosure`	keyword	yes	—	Enclosure measurement.
`-opposite_side`	flag	yes	—	Opposite-side mode.
`licon_poly`	layer	yes	—	Inner/reference feature.
`POLY`	layer	yes	—	Enclosing layer.
`-lt <float_value>`	flag+number	yes	—	Comparator threshold.

Example Usage.

```
enclosure -opposite\_side <layer1\_name> <layer2\_name> -lt <float\_value>
```

1.16 density_rule "min_fail" ...

Description.

density_rule declares a sliding-window density analysis. With a min_fail profile, the engine reports windows whose coverage falls below density_minimum. The window is defined by density_window and slid across the design by density_step. Optional density_exclude regions are subtracted from the analysis area to avoid false positives (e.g., over large blockage shapes).

Manufacturing motivations: insufficient pattern density can cause CMP dishing, erosion, and non-uniformity in lithography. Foundry decks therefore enforce lower bounds per layer and sometimes per direction. The density_surround adds a margin (halo) around the evaluation window to account for proximity effects. density_mode TEST selects a diagnostic mode; density_report assigns a tagged name to the output report to organize multiple analyses in a run.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
density_rule ¨min_fail¨	block	yes	—	Begin density block.
density_layer <layer_name>	layer	yes	—	Layer to analyze.
density_window SIZE <int> BY <int>	window	yes	—	Window size (DB units or um).
density_step <int>	number	optional	—	Stride between adjacent windows.
density_exclude <layer>	layer	optional	—	Subtract from analysis area.
density_maximum <float>	number	optional	1.0	Upper bound (rarely used for min_fail).
density_minimum <float>	number	optional	—	Lower bound for pass.
density_surround <int>	number	optional	0	Halo around window.
density_mode TEST	enum	optional	DEFAULT	Analysis mode.
density_report <string>	string	optional	—	Named report id.
density_min_fail	flag	optional	—	Emit min-density failures.

Example Usage.

```
density\_rule "min\_fail" {
  density\_layer <layer1\_name>
```

```
  density\_window SIZE <int\_value> BY <int\_value>
  density\_step <int\_value>
  density\_exclude <layer2\_name>
  density\_maximum <float\_value>
  density\_minimum <float\_value>
  density\_surround <int\_value>
  density\_mode TEST
  density\_report <string\_id>
  density\_min\_fail
}
```

1.17 density_rule "max_fail" ...

Description.

This density profile flags windows that exceed the maximum threshold or fall outside a permitted range. Directional flags (density_xdir_fail, density_ydir_fail) partition the design into directional slices to capture anisotropy (e.g., long metals preferentially oriented in X). density_out_of_range reports any window below minimum or above maximum, depending on previously declared bounds (from another density block or defaults).

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`density_rule "max_fail"`	block	yes	—	Begin density block.
`density_maximum <float>`	number	optional	—	Upper bound for pass.
`density_max_fail`	flag	optional	—	Emit max-density failures.
`density_out_of_range`	flag	optional	—	Emit if below min or above max.
`density_xdir_fail`	flag	optional	—	Directional failure in X.
`density_ydir_fail`	flag	optional	—	Directional failure in Y.

Example Usage.

```
density\_rule "max\_fail" {
  density\_maximum <float\_value>
  density\_out\_of\_range
  density\_xdir\_fail
  density\_ydir\_fail
  density\_max\_fail
}
```

1.18 get_intersecting -neg npc poly_licon

Description.

With the -neg modifier, get_intersecting returns shapes from the first operand that do *not* intersect the second operand. For npc vs. poly_licon, this isolates nitride-poly-cut shapes that are clear of poly contacts—useful to find missing or misaligned contacts, or to assert keep-out spacing from contact regions.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_intersecting	keyword	yes	—	Intersection-based filter.
-neg	flag	optional	off	Invert selection (A minus intersect(A,B)).
npc	layer	yes	—	Primary set.
poly_licon	layer	yes	—	Intersect-with set.

Example Usage.

```
get\_intersecting -neg <layer1\_name> <layer2\_name>
```

1.19 get_intersecting npc poly_licon

Description.

Standard intersection of nitride-poly-cut with poly contacts. Use to drive enclosure of poly around contacts, or to verify that only intended poly regions are cut.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_intersecting	keyword	yes	—	Filter A by intersection with B.
npc	layer	yes	—	Primary set.
poly_licon	layer	yes	—	Intersect-with set.

Example Usage.

```
get\_intersecting <layer1\_name> <layer2\_name>
```

1.20 get_intersecting -neg npc poly_licon -layerOut somelayer

Description.

Same as the negative-intersection rule, but the result is materialized for review and reuse. Persisting the subset aids visualization and simplifies subsequent rule blocks that reference the same derived geometry.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
get_intersecting	keyword	yes	—	Filter based on (non-)intersection.
-neg	flag	yes	on	Return shapes in A that do not intersect B.
npc	layer	yes	—	Primary set.
poly_licon	layer	yes	—	Second set.
-layerOut <output_layer>	flag+layer	yes	—	Output layer.

Example Usage.

```
get\_intersecting -neg <layer1\_name> <layer2\_name> -layerOut <output\_layer>
```

1.21 `lvr_layer_map 235 -datatype 4 30000`

Description.

Maps a source GDS/OAS layer number and datatype to an internal LVR layer id. This decouples foundry-specific stream assignments from rule logic and lets the deck use semantic names elsewhere. Multiple mappings can target the same internal id to aggregate equivalent inputs (e.g., OPC variants).

Conflicts should be avoided: mapping the same (layer,datatype) pair twice to different ids is undefined. If `-datatype` is omitted, a default (often 0) is assumed. Use explicit mapping entries to ensure robust import across design libraries and PDK revisions.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`lvr_layer_map`	keyword	yes	—	Create mapping entry.
`<int_layer>`	number	yes	—	Source stream layer.
`-datatype <int>`	flag+number	optional	0	Source datatype.
`<int_id>`	number	yes	—	Internal LVR layer id.

Example Usage.

```
lvr\_layer\_map <int\_layer> -datatype <int\_value> <int\_id>
```

1.22 `lvr_layer_map 74 -texttype 5 30320`

Description.

Like `lvr_layer_map` for geometry, this variant maps source text layers by `texttype`. Text layers are used for labels, pin names, or markers that participate in LVS and annotation flows. Mapping ensures consistent ingestion of text semantics across libraries.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
lvr_layer_map	keyword	yes	—	Create mapping entry.
<int_layer>	number	yes	—	Source text layer.
-texttype <int>	flag+number	yes	—	Source text type.
<int_id>	number	yes	—	Internal text layer id.

Example Usage.

```
lvr\_layer\_map <int\_layer> -texttype <int\_value> <int\_id>
```

1.23 `lvr_layer_def BOUND 30000`

Description.

Defines a symbolic alias for an internal layer id. Whereas `lvr_layer_map` binds external stream codes to internal ids, `lvr_layer_def` binds human-readable names (e.g., `BOUND`) to those ids for use elsewhere in the deck. This improves readability and allows refactoring without touching numerical ids.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
lvr_layer_def	keyword	yes	—	Define alias.
<layer_alias>	string	yes	—	Symbolic layer name.
<int_id>	number	yes	—	Existing internal id.

Example Usage.

```
lvr\_layer\_def <layer\_alias> <int\_id>
```

1.24 `connect layer1 layer2`

Description.

Declares physical/electrical connectivity between two layers. The most common use is to connect conductor layers via a via/contact layer (e.g., `M1` connected to `M2` through `V1`). Connectivity declarations build the graph that LVS uses to compute nets from geometry.

Connections are undirected and typically transitive: if A is connected to B and B to C, then A is connected to C. The order of declarations does not matter, but the graph must remain acyclic with respect to purpose (no layer should be both a via and a conductor simultaneously). Some flows also support conditional connect (e.g., within device recognition regions) for advanced extraction control.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`connect`	keyword	yes	—	Declare connectivity.
`<layer1_name>`	layer	yes	—	First layer.
`<layer2_name>`	layer	yes	—	Second layer.

Example Usage.

```
connect <layer1\_name> <layer2\_name>
```

1.25 `lvs_timeout 10`

Description.

Sets a wall-clock timeout (seconds) applied to LVS phases such as device recognition, graph matching, or equivalence checking. Timeouts are safeguards for pathological cases (e.g., degenerate hierarchies or mismatched black boxes).

When a timeout elapses, the engine should fail gracefully and record the scope in the report. Use conservative values to avoid masking genuine issues; prefer granular timeouts per phase rather than a single global ceiling when available.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`lvs_timeout`	keyword	yes	—	Set timeout policy.
`<int_value>`	number (s)	yes	—	Timeout in seconds.

Example Usage.

```
lvs\_timeout <int\_value>
```

1.26 caption "dnwell.2 : min. dnwell width : 3.0um"

Description.

Assigns a human-readable label to the next emitted markers or to the immediately following rule block (e.g., a `drc_rule`). Captions convey intent to designers and appear in reports, marker browsers, or GUIs.

Good captions include the rule id, a short description, and the key threshold (e.g., minimum width). Keep them stable across deck revisions to maintain traceability between runs.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
caption	keyword	yes	—	Attach label to following rule(s).
¨<free_text>¨	string	yes	—	Caption text.

Example Usage.

```
caption \"<rule\_id> : <short\_description> : <float\_value>um\"
```

1.27 drc_rule "dnwell.2"

Description.

Opens a DRC rule block for checks associated with the logical caption "dnwell.2". Within this block, exactly one primitive check is typically placed, preceded by a human-readable caption. Using a consistent caption unifies report text, marker browser labels, and documentation references. Rule authors often keep one check per block to simplify debug and per-rule enable/disable.

The block does not by itself enforce any geometry constraint; semantics come from the enclosed primitive (e.g., edge_width, spacing). The wrapper standardizes output formatting and makes downstream parsing predictable. When multiple similar checks are needed, duplicate the block with distinct captions (e.g., "dnwell.2a", "dnwell.2b") to keep markers disambiguated.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`drc_rule {`	block opener	yes	—	Begins the rule block.
`caption "dnwell.2"`	string	yes	—	Human-readable tag shown in reports/markers.
`<drc_rule>`	line	yes	—	The actual check (see entries below).
`}`	block closer	yes	—	Ends the rule block.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  <drc_rule>
}
```

1.28 edge_width DNWELL -lt 3.0

Description.

Checks that the edge-based width of shapes on DNWELL is strictly less than 3.0. In a “minimum width” specification, decks commonly encode a fail when width is *less than* the minimum, so this primitive is used with the block’s caption/reporting to flag sub-minimum wells. Edge-width measurement follows the engine’s definition (e.g., medial-axis or offset-based), which should be consistent across layers to avoid bias near corners and notches.

Corner rounding and grid quantization may slightly perturb measured widths near acute features; sign-off flows typically heal slivers or snap to a manufacturing grid before measurement to stabilize results across variants.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`edge_width`	keyword	yes	—	Measures polygon edge-based width.
`DNWELL`	layer	yes	—	Target layer to measure.
`-lt 3.0`	flag+number	yes	—	Width must be $<$ the threshold.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  edge_width DNWELL -lt 3.0
}
```

1.29 `edge_width DNWELL -lt 3.0` **(duplicate)**

Description.

This is a separate, duplicate entry documented independently (no grouping), to allow distinct reporting or future threshold tuning while preserving the same caption context.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`edge_width`	keyword	yes	—	Same semantics as prior entry.
`DNWELL`	layer	yes	—	Target layer.
`-lt 3.0`	flag+number	yes	—	Threshold repeated intentionally.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  edge_width DNWELL -lt 3.0
}
```

1.30 edge_width DNWELL -gt 3.0

Description.

Checks that the edge-based width of DNWELL is strictly greater than 3.0. This can be used for “maximum-width” or “forbidden narrow channel” style constraints depending on deck policy. Use with caution alongside the -lt variant to avoid contradictory requirements.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`edge_width`	keyword	yes	—	Edge-based width metric.
`DNWELL`	layer	yes	—	Target layer.
`-gt 3.0`	flag+number	yes	—	Width must be $>$ the threshold.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  edge_width DNWELL -gt 3.0
}
```

1.31 `extension DNWELL DNWELL -eq 0`

Description.

Checks that the extension between the two operands is exactly zero (abutment). For self-operand use, this often validates that adjacent `DNWELL` instances either do not overlap or meet perfectly without overhangs. Exact-equal tests are sensitive to grid/rounding; prefer normalized database units and healed boundaries to reduce false flags on coincident edges.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`extension`	keyword	yes	—	Edge/endpoint extension metric.
`DNWELL`	layer	yes	—	First operand.
`DNWELL`	layer	yes	—	Second operand.
`-eq 0`	flag+number	yes	—	Exact equality (use healed geometry).

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  extension DNWELL DNWELL -eq 0
}
```

1.32 `extension DNWELL DNWELL -lt 0.1`

Description.

Checks that the extension between the two operands is strictly less than `0.1`. This is useful to cap overhangs or near-abutment allowances where slight overlaps are permitted but bounded.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`extension`	keyword	yes	—	Extension metric between operands.
`DNWELL`	layer	yes	—	First operand.
`DNWELL`	layer	yes	—	Second operand.
`-lt 0.1`	flag+number	yes	—	Threshold for “less-than” constraint.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  extension DNWELL DNWELL -lt 0.1
}
```

1.33 edge_length MF -lt 7.2

Description.

Checks that the measured edge length (contour length of shapes) on layer MF is strictly less than 7.2. Depending on engine semantics, this can target short-edge constraints or be repurposed to gate patterns that should not form excessively short segments.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`edge_length`	keyword	yes	—	Measures perimeter segment length(s).
`MF`	layer	yes	—	Target layer.
`-lt 7.2`	flag+number	yes	—	Edge length must be $<$ threshold.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  edge_length MF -lt 7.2
}
```

1.34 `area MET3 -lt 0.24`

Description.

Checks that the polygon area on `MET3` is strictly less than `0.24`. This is typically used to catch undersized features or enforce minimum-area constraints by flagging shapes below a required floor.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`area`	keyword	yes	—	Computes polygon area.
`MET3`	layer	yes	—	Target layer.
`-lt 0.24`	flag+number	yes	—	Area must be $<$ threshold.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  area MET3 -lt 0.24
}
```

1.35 `area MET3 -lt 0.24 -layerOut temp`

Description.

Same as the previous area check, but the resulting fail/diagnostic regions are materialized to output layer `temp` for visualization and reuse in follow-on debug rules. The exact contents (fail shapes, measured clips, or references) depend on engine policy.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`area`	keyword	yes	—	Polygon area evaluation.
`MET3`	layer	yes	—	Target layer.
`-lt 0.24`	flag+number	yes	—	Area must be $<$ threshold.
`-layerOut temp`	flag+layer	yes	—	Sends result to `temp`.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  area MET3 -lt 0.24 -layerOut temp
}
```

1.36 `spacing -wider 1.5 -longer 4.0 -same_layer metal8 metal8 -lt 1.5`

Description.

Same-layer spacing check on `metal8` with qualifiers: `-wider 1.5` indicates that shapes wider than this value are considered in the spacing context; `-longer 4.0` similarly filters by length. The `-same_layer metal8 metal8` scope restricts measurement to intra-layer pairs. The `-lt 1.5` comparator enforces a minimum spacing of `1.5` (violations where spacing falls below the threshold).

Qualifier semantics (width/length measurement axes) follow the engine and PDK conventions; ensure the deck's global grid/angle settings match routing style.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`spacing`	keyword	yes	—	Spacing/edge-to-edge measurement.
`-wider 1.5`	flag+number	no	—	Consider only shapes wider than value.
`-longer 4.0`	flag+number	no	—	Consider only shapes longer than value.
`-same_layer metal8 metal8`	scope	yes	—	Intra-layer spacing on `metal8`.
`-lt 1.5`	flag+number	yes	—	Spacing must be ge$threshold; fails when$¡.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  spacing -wider 1.5 -longer 4.0 -same_layer metal8 metal8 -lt 1.5
}
```

1.37 spacing -same_layer DNWELL DNWELL -lt 6.3

Description.

Same-layer spacing check on DNWELL polygons. The comparator flags any pair of well shapes that violate the minimum separation of 6.3.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`spacing`	keyword	yes	—	Edge-to-edge spacing measurement.
`-same_layer DNWELL DNWELL`	scope	yes	—	Intra-layer well-to-well spacing.
`-lt 6.3`	flag+number	yes	—	Spacing must be ge$threshold; fails when¡$.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  spacing -same_layer DNWELL DNWELL -lt 6.3
}
```

1.38 `spacing LVTN HVTP -lt 0.38`

Description.

Inter-layer spacing check between `LVTN` and `HVTP`. This captures proximity requirements across two different implant or threshold-related layers. The comparator encodes the minimum allowed separation; pairs closer than the threshold are reported as violations.

Syntax and Arguments.

Parameter	Type	Required	Default	Notes
`spacing`	keyword	yes	—	Inter-layer spacing measurement.
`LVTN`	layer	yes	—	First layer operand.
`HVTP`	layer	yes	—	Second layer operand.
`-lt 0.38`	flag+number	yes	—	Spacing must be ge$threshold; fails when$¡.

Example Usage.

```
drc_rule "rule_name" {
  caption "dnwell.2"
  spacing LVTN HVTP -lt 0.38
}
```

2 LRF File Examples

2.1 SKY130.lrf Example

```
lvr_layer_map 235 -datatype 4 30000
lvr_layer_def BOUND 30000
lvr_layer_map 64 -datatype 18 30005
lvr_layer_def DNWELL 30005
lvr_layer_map 64 -datatype 13 30010
lvr_layer_def PWRES 30010
lvr_layer_map 64 -datatype 20 30015
lvr_layer_def NWELL 30015
lvr_layer_map 64 -texttype 5 30020
lvr_layer_def NWELLTXT 30020
lvr_layer_map 64 -datatype 16 30025
lvr_layer_def NWELLPIN 30025
lvr_layer_map 122 -texttype 5 30030
lvr_layer_def SUBTXT 30030
lvr_layer_map 64 -texttype 59 30035
lvr_layer_def SUBPIN 30035
lvr_layer_map 65 -datatype 20 30040
lvr_layer_def DIFF 30040
lvr_layer_map 65 -datatype 44 30045
lvr_layer_def TAP 30045
lvr_layer_map 94 -datatype 20 30050
lvr_layer_def PSDM 30050
```

```
lvr_layer_map 93 -datatype 44 30055
lvr_layer_def NSDM 30055
lvr_layer_map 125 -datatype 44 30060
lvr_layer_def LVTN 30060
lvr_layer_map 18 -datatype 20 30065
lvr_layer_def HVTR 30065
lvr_layer_map 78 -datatype 44 30070
lvr_layer_def HVTP 30070
lvr_layer_map 80 -datatype 20 30075
lvr_layer_def SONOS 30075
lvr_layer_map 81 -datatype 2 30080
lvr_layer_def COREID 30080
lvr_layer_map 81 -datatype 4 30085
lvr_layer_def STDCELL 30085
lvr_layer_map 82 -datatype 20 30090
lvr_layer_def NPNID 30090
lvr_layer_map 82 -datatype 44 30095
lvr_layer_def PNPID 30095
lvr_layer_map 86 -datatype 20 30100
lvr_layer_def RPM 30100
lvr_layer_map 79 -datatype 20 30105
lvr_layer_def URPM 30105
lvr_layer_map 11 -datatype 44 30110
lvr_layer_def LDNTM 30110
lvr_layer_map 125 -datatype 20 30115
lvr_layer_def HVNTM 30115
lvr_layer_map 66 -datatype 20 30120
lvr_layer_def POLY 30120
lvr_layer_map 66 -texttype 5 30125
lvr_layer_def POLYTXT 30125
lvr_layer_map 66 -datatype 16 30130
lvr_layer_def POLYPIN 30130
lvr_layer_map 75 -datatype 20 30135
lvr_layer_def HVI 30135
lvr_layer_map 66 -datatype 44 30140
lvr_layer_def LICON 30140
lvr_layer_map 95 -datatype 20 30145
lvr_layer_def NPC 30145
lvr_layer_map 65 -datatype 13 30150
lvr_layer_def DIFFRES 30150
lvr_layer_map 66 -datatype 13 30155
lvr_layer_def POLYRES 30155
lvr_layer_map 66 -datatype 15 30160
lvr_layer_def POLYSHO 30160
lvr_layer_map 81 -datatype 23 30165
lvr_layer_def DIODE 30165
lvr_layer_map 67 -datatype 20 30170
lvr_layer_def LI 30170
lvr_layer_map 67 -texttype 5 30175
lvr_layer_def LITXT 30175
lvr_layer_map 67 -datatype 16 30180
lvr_layer_def LIPIN 30180
lvr_layer_map 67 -datatype 13 30185
lvr_layer_def LIRES 30185
lvr_layer_map 67 -datatype 44 30190
lvr_layer_def MCON 30190
lvr_layer_map 68 -datatype 20 30195
lvr_layer_def MET1 30195
lvr_layer_map 68 -texttype 5 30200
lvr_layer_def MET1TXT 30200
lvr_layer_map 68 -datatype 16 30205
lvr_layer_def MET1PIN 30205
```

```
lvr_layer_map 68 -datatype 13 30210
lvr_layer_def MET1RES 30210
lvr_layer_map 68 -datatype 44 30215
lvr_layer_def VIA1 30215
lvr_layer_map 69 -datatype 20 30220
lvr_layer_def MET2 30220
lvr_layer_map 69 -texttype 5 30225
lvr_layer_def MET2TXT 30225
lvr_layer_map 69 -datatype 16 30230
lvr_layer_def MET2PIN 30230
lvr_layer_map 69 -datatype 13 30235
lvr_layer_def MET2RES 30235
lvr_layer_map 69 -datatype 44 30240
lvr_layer_def VIA2 30240
lvr_layer_map 70 -datatype 20 30245
lvr_layer_def MET3 30245
lvr_layer_map 70 -texttype 5 30250
lvr_layer_def MET3TXT 30250
lvr_layer_map 70 -datatype 16 30255
lvr_layer_def MET3PIN 30255
lvr_layer_map 70 -datatype 13 30260
lvr_layer_def MET3RES 30260
lvr_layer_map 70 -datatype 44 30265
lvr_layer_def VIA3 30265
lvr_layer_map 71 -datatype 20 30270
lvr_layer_def MET4 30270
lvr_layer_map 71 -texttype 5 30275
lvr_layer_def MET4TXT 30275
lvr_layer_map 71 -datatype 16 30280
lvr_layer_def MET4PIN 30280
lvr_layer_map 71 -datatype 13 30285
lvr_layer_def MET4RES 30285
lvr_layer_map 71 -datatype 44 30290
lvr_layer_def VIA4 30290
lvr_layer_map 72 -datatype 20 30295
lvr_layer_def MET5 30295
lvr_layer_map 72 -texttype 5 30300
lvr_layer_def MET5TXT 30300
lvr_layer_map 72 -datatype 16 30305
lvr_layer_def MET5PIN 30305
lvr_layer_map 72 -datatype 13 30310
lvr_layer_def MET5RES 30310
lvr_layer_map 74 -datatype 20 30315
lvr_layer_def RDL 30315
lvr_layer_map 74 -texttype 5 30320
lvr_layer_def RDLTXT 30320
lvr_layer_map 74 -datatype 16 30325
lvr_layer_def RDLPIN 30325
lvr_layer_map 76 -datatype 20 30330
lvr_layer_def GLASS 30330
lvr_layer_map 89 -datatype 44 30335
lvr_layer_def CAPM 30335
lvr_layer_map 97 -datatype 44 30340
lvr_layer_def CAPM2 30340
lvr_layer_map 81 -datatype 14 30345
lvr_layer_def LOWTAPD 30345
lvr_layer_map 62 -datatype 24 30350
lvr_layer_def FILLOBSM1 30350
lvr_layer_map 105 -datatype 52 30355
lvr_layer_def FILLOBSM2 30355
lvr_layer_map 107 -datatype 24 30360
lvr_layer_def FILLOBSM3 30360
```

```
lvr_layer_map 112 -datatype 4 30365
lvr_layer_def FILLOBSM4 30365
lvr_layer_map 92 -datatype 44 30370
lvr_layer_def NCM 30370
lvr_layer_map 236 -datatype 0 30375
lvr_layer_def SUB 30375



lvr_layer_map 61 -datatype 20 30380
lvr_layer_def NSM 30380
lvr_layer_map 89 -datatype 44 30385
lvr_layer_def CAPM 30385
lvr_layer_map 97 -datatype 44 30390
lvr_layer_def CAP2M 30390
lvr_layer_map 74 -datatype 21 30395
lvr_layer_def VHVI 30395
lvr_layer_map 74 -datatype 22 30400
lvr_layer_def UHVI 30400
lvr_layer_map 82 -datatype 20 30405
lvr_layer_def NPN 30405
lvr_layer_map 82 -datatype 24 30410
lvr_layer_def INDUCTOR 30410
lvr_layer_map 82 -datatype 64 30415
lvr_layer_def VPP 30415
lvr_layer_map 82 -datatype 44 30420
lvr_layer_def PNP 30420
lvr_layer_map 84 -datatype 44 30425
lvr_layer_def LVS_PRUNE 30425
lvr_layer_map 92 -datatype 44 30430
lvr_layer_def NCM 30430
lvr_layer_map 81 -datatype 20 30435
lvr_layer_def PADCENTER 30435
lvr_layer_map 76 -datatype 44 30440
lvr_layer_def MF 30440
lvr_layer_map 81 -datatype 1 30445
lvr_layer_def AREAID_SL 30445
lvr_layer_map 81 -datatype 2 30450
lvr_layer_def AREAID_CE 30450
lvr_layer_map 81 -datatype 3 30455
lvr_layer_def AREAID_FE 30455
lvr_layer_map 81 -datatype 4 30460
lvr_layer_def AREAID_SC 30460
lvr_layer_map 81 -datatype 6 30465
lvr_layer_def AREAID_SF 30465
lvr_layer_map 81 -datatype 7 30470
lvr_layer_def AREAID_SW 30470
lvr_layer_map 81 -datatype 8 30475
lvr_layer_def AREAID_SR 30475
lvr_layer_map 81 -datatype 10 30480
lvr_layer_def AREAID_MT 30480
lvr_layer_map 81 -datatype 11 30485
lvr_layer_def AREAID_DT 30485
lvr_layer_map 81 -datatype 12 30490
lvr_layer_def AREAID_FT 30490
lvr_layer_map 81 -datatype 13 30495
lvr_layer_def AREAID_WW 30495
lvr_layer_map 81 -datatype 14 30500
lvr_layer_def AREAID_LD 30500
lvr_layer_map 81 -datatype 15 30505
lvr_layer_def AREAID_NS 30505
lvr_layer_map 81 -datatype 17 30510
```

```
lvr_layer_def AREAID_IJ 30510
lvr_layer_map 81 -datatype 18 30515
lvr_layer_def AREAID_ZR 30515
lvr_layer_map 81 -datatype 19 30520
lvr_layer_def AREAID_ED 30520
lvr_layer_map 81 -datatype 23 30525
lvr_layer_def AREAID_DE 30525
lvr_layer_map 81 -datatype 24 30530
lvr_layer_def AREAID_RD 30530
lvr_layer_map 81 -datatype 50 30535
lvr_layer_def AREAID_DN 30535
lvr_layer_map 81 -datatype 51 30540
lvr_layer_def AREAID_CR 30540
lvr_layer_map 81 -datatype 52 30545
lvr_layer_def AREAID_CD 30545
lvr_layer_map 81 -datatype 53 30550
lvr_layer_def AREAID_ST 30550
lvr_layer_map 81 -datatype 54 30555
lvr_layer_def AREAID_OP 30555
lvr_layer_map 81 -datatype 57 30560
lvr_layer_def AREAID_EN 30560
lvr_layer_map 81 -datatype 58 30565
lvr_layer_def AREAID_EN20 30565
lvr_layer_map 81 -datatype 60 30570
lvr_layer_def AREAID_LE 30570
lvr_layer_map 81 -datatype 63 30575
lvr_layer_def AREAID_HL 30575
lvr_layer_map 81 -datatype 70 30580
lvr_layer_def AREAID_SD 30580
lvr_layer_map 81 -datatype 81 30585
lvr_layer_def AREAID_PO 30585
lvr_layer_map 81 -datatype 84 30590
lvr_layer_def AREAID_IT 30590
lvr_layer_map 81 -datatype 101 30595
lvr_layer_def AREAID_ET 30595
lvr_layer_map 81 -datatype 108 30600
lvr_layer_def AREAID_LVT 30600
lvr_layer_map 81 -datatype 125 30605
lvr_layer_def AREAID_RE 30605
lvr_layer_map 81 -datatype 79 30610
lvr_layer_def AREAID_AG 30610
lvr_layer_map 66 -datatype 13 30615
lvr_layer_def POLY_RS 30615
lvr_layer_map 65 -datatype 13 30620
lvr_layer_def DIFF_RS 30620
lvr_layer_map 64 -datatype 13 30625
lvr_layer_def PWELL_RS 30625
lvr_layer_map 67 -datatype 13 30630
lvr_layer_def LI_RS 30630
lvr_layer_map 22 -datatype 20 30635
lvr_layer_def CFOM 30635


size ( extent ) -by 1.0 -layerOut bulk

not bulk NWELL -layerOut PWELL
and DIFF NSDM -layerOut NDIFF
and DIFF PSDM -layerOut PDIFF
and PDIFF POLY -layerOut PGATE
and NDIFF POLY -layerOut NGATE
not PDIFF PGATE -layerOut PSD
not NDIFF NGATE -layerOut NSD
```

```
//not MYDIFF1 PGATE -layerOut MYDIFF2
//not MYDIFF2 NGATE -layerOut MYDIFF
or PSD NSD -layerOut MYDIFF
or POLY POLY -layerOut MYPOLY
//not POLY PGATE -layerOut POLY1
//not POLY1 NGATE -layerOut MYPOLY


connect LI  LI
connect MET1  MET1
//connect MYDIFF MYDIFF
//connect PDIFF PDIFF
//connect NDIFF NDIFF
//connect PSD PSD
//connect NSD NSD
//connect POLY POLY
//connect MET1  MET1TXT
//connect MET2  MET2
//connect MET3  MET3
//connect MET4  MET4
//connect MET5  MET5
//connect NWELL NWELL
//connect NWELL NWELLTXT
//connect SUB SUB
//connect SUB SUBPIN
//connect SUB SUBTXT
connect VIA2 MET3
connect MET2 VIA2
connect VIA1 MET2
connect MET1 VIA1
connect MCON MET1
connect LI MCON
connect LICON LI
connect MYDIFF LICON
connect MYPOLY LICON
//connect PSD LICON
//connect NSD LICON
//connect POLY LICON
//connect NWELL LICON
//connect SUB TAP
//connect bulk TAP
//connect NGATE POLY
//connect PGATE POLY
//connect PWELL SUB


lvs_timeout 10
lvs_max_error 100
lvs_ground_pin VNB
lvs_ground_pin VSS
lvs_ground_pin VGND
lvs_power_pin VPWR
lvs_power_pin VPB
lvs_power_pin VDD
//lvs_waiver_netlist_net  Ab1
//lvs_waiver_netlist_net  VGND
//lvs_waiver_netlist_net  net105
//lvs_waiver_netlist_net  smdNA0218
//lvs_waiver_netlist_net  sndNS
//lvs_waiver_netlist_net  xlow
//lvs_waiver_netlist_net  SOb12
```

```
lvs_power_pin1 VDD
lvs_power_pin2 VDD
lvs_power_pin3 VDD
lvs_power_pin4 VDD
lvs_power_pin5 VDD
lvs_power_pin6 VDD
lvs_power_pin7 VDD

  drc_rule "dnwell.2" {
    caption "dnwell.2 : min. dnwell width : 3.0um"
    edge_width DNWELL -lt 3.0
  }

  drc_rule "dnwell.3" {
    caption "dnwell.3 : min. dnwell spacing : 6.3um"
    spacing -same_layer DNWELL DNWELL -lt 6.3
  }

  drc_rule "dnwell.4" {
    caption "dnwell.4 : dnwell must not overlap pnp"
    and DNWELL PNP
  }

  drc_rule "dnwell.5" {
    caption "p+ must not straddle dnwell"
    extension DNWELL DNWELL -eq 0
  }

  drc_rule "nwell.1" {
    caption "nwell.1 : min. nwell width : 0.84um"
    edge_width NWELL -lt 0.84
  }

  drc_rule "nwell.2a" {
    caption "nwell.2a : min. nwell spacing (merged if less) : 1.27um"
    spacing -same_layer NWELL NWELL -lt 1.27
  }

  drc_rule "nwell.4" {
    caption "nwell4 : all nwell exempt inside uhvi must contain a n+tap"
    not NWELL UHVI
  }

  drc_rule "nwell.5" {
    caption "nwell.5 : min. nwell enclosing dnwell exempt unside uhvi : 0.4um"
    enclosure -all_side NWELL DNWELL -lt 0.4
  }

  drc_rule "nwell.6" {
    caption "nwell.6 : min. dnwell enclosing nwell exempt unside uhvi : 1.03um"
    enclosure -all_side NWELL DNWELL -lt 1.03
  }

  drc_rule "pwbm" {
    caption "pwbm must be inside uhvi"
    not PWBM UHVI
  }

  drc_rule "pwbm.4" {
    caption "pwbm.4 : dnwell inside uhvi must be enclosed by pwbm"
    not PWBM DNWELL
  }
```

```
drc_rule "pwdem.3" {
  caption "pwdem.3 : pwde must be inside pwbm"
  not PWDEM PWBM
}

drc_rule "pwdem.4" {
  caption "pwdem.4 : pwde must be inside uhvi"
  not PWDEM UHVI
}

drc_rule "pwdem.5" {
  caption "pwdem.5 : pwde must be inside dnwell"
  not PWDEM DNWELL
}

drc_rule "hvtp" {
  caption "hvtp must inside nwell"
  and NWELL HVTP -layerOut AB
  not AB HVTP
}

drc_rule "hvtp.1" {
  caption "hvtp.1 : min. hvtp width : 0.38um"
  edge_width HVTP -lt 0.38
}

drc_rule "hvtp.2" {
  caption "hvtp.2 : min. hvtp spacing : 0.38um"
  spacing -same_layer HVTP HVTP -lt 0.38
}

drc_rule "hvtp.3" {
  caption "hvtp.3 : min. hvtp enclosure of pfet gate : 0.18um"
  //enclosure -all_side PGATE HVTP -lt 0.18
  //TODO
}

drc_rule "hvtp.4" {
  caption "hvtp.4 : min. hvtp spacing pfet gate: 0.18um"
  spacing -same_layer HVTP HVTP -lt 0.18
}

drc_rule "hvtp.5" {
  caption "hvtp.5 : min. hvtp area : 0.265um²"
  area HVTP -lt 0.265
}

drc_rule "hvtr.1" {
  caption "hvtr.1 : min. hvtr width : 0.38um"
  edge_width HVTR -lt 0.38
}

drc_rule "hvtr.2" {
  caption "hvtr.2 : min. hvtr spacing : 0.38um"
  spacing -same_layer HVTR HVTR -lt 0.38
}

drc_rule "lvtn.1" {
  caption "lvtn.1 : min. lvtn width : 0.38um"
  edge_width LVTN -lt 0.38
}
```

```
drc_rule "lvtn.2" {
  caption "lvtn.2 : min. lvtn spacing : 0.38um"
  spacing -same_layer LVTN LVTN -lt 0.38
}

drc_rule "lvtn.3a" {
  caption "lvtn.3a : min. lvtn spacing to gate : 0.18um"
  spacing -same_layer LVTN LVTN -lt 0.18
}

drc_rule "lvtn.3b" {
  caption "lvtn.3b : min. lvtn spacing to pfet s/d : 0.18um"
  spacing -same_layer LVTN LVTN -lt 0.18
}

drc_rule "lvtn.4b" {
  caption "lvtn.4b : min. lvtn enclosing to gate : 0.18um"
  enclosure -all_side PGATE LVTN -lt 0.18
  enclosure -all_side NGATE LVTN -lt 0.18
}

drc_rule "lvtn.9" {
  caption "lvtn.9 : min. lvtn spacing hvtp : 0.38um"
  spacing LVTN HVTP -lt 0.38
}

drc_rule "lvtn.4b" {
  caption "lvtn.4b : min. lvtn enclosure of gate : 0.18um"
  enclosure -all_side PGATE LVTN -lt 0.18
  enclosure -all_side NGATE LVTN -lt 0.18
}

drc_rule "lvtn.12" {
  caption "lvtn.12 : min. lvtn spacing nwell inside areaid.ce : 0.38um"
  spacing LVTN NWELL -lt 0.38
}

drc_rule "lvtn.13" {
  caption "lvtn.13 : min. lvtn area : 0.265um²"
  area LVTN -lt 0.265
}

drc_rule "ncm.x.3" {
  caption "ncm.x.3 : ncm must not overlap n+diff"
  and NCM NCM
}

drc_rule "ncm.1" {
  caption "ncm.1 : min. ncm width : 0.38um"
  edge_width NCM -lt 0.38
}

drc_rule "ncm.2" {
  caption "ncm.2 : min. ncm spacing manual merge if smaller : 0.38um"
  spacing -same_layer NCM NCM -lt 0.38
}

drc_rule "ncm.3" {
  caption "ncm.3 : min. ncm enclosure of p+diff : 0.18um"
  enclosure -all_side PDIFF NCM -lt 0.18
}
```

```
drc_rule "ncm.5" {
  caption "ncm.5 : min. ncm spacing lvtn diff : 0.23um"
  spacing NCM LVTN -lt 0.23
}

drc_rule "ncm.6" {
  caption "ncm.6 : min. ncm spacing nfet : 0.2um"
  spacing -same_layer NCM NCM -lt 0.2
}

drc_rule "ncm.7" {
  caption "ncm.13 : min. ncm area : 0.265um²"
  area NCM -lt 0.265
}

drc_rule "difftap.1" {
  caption "difftap.1 : min. difftap width : 0.15um"
  edge_width DIFFTAP -lt 0.15
}

drc_rule "difftap.2" {
  caption "difftap.2: min. gate (exempt areaid.sc) width : 0.42um"
  edge_width DIFFTAP -lt 0.42
}

drc_rule "difftap.2" {
  caption "difftap.2: min. gate inside areaid.sc width : 0.36um"
  not DIFFTAP DIFFTAP
}

drc_rule "difftap.3" {
  caption "difftap.3 : min. difftap spacing : 0.27um"
  spacing -same_layer DIFFTAP DIFFTAP -lt 0.27
}

drc_rule "difftap.7" {
  caption "difftap.7 : min. diff/tap spacing to non-coincident diff edge : 0.13um"
  spacing -same_layer DIFFTAP DIFFTAP -lt 0.13
}

drc_rule "difftap.7" {
  caption "difftap.7 : min. diff/tap spacing to non-coincident tap edge : 0.13um"
  spacing -same_layer  DIFFTAP DIFFTAP -lt 0.13
}

drc_rule "difftap.8" {
  caption "difftap.8 : min. p+diff enclosure by nwell : 0.18um"
  enclosure -all_side DIFFTAP NWELL -lt 0.18
}

drc_rule "difftap.9" {
  caption "difftap.9 : min. n+diff spacing to nwell : 0.34um"
  spacing DIFFTAP NWELL -lt 0.34
}

drc_rule "difftap.10" {
  caption "difftap.10 : min. n+tap enclosure by nwell : 0.18um"
  enclosure -all_side DIFFTAP NWELL -lt 0.18
}

drc_rule "difftap.11" {
```

```
  caption "difftap.11 : min. p+tap spacing to nwell : 0.13um"
  spacing DIFFTAP NWELL -lt 0.13
}

drc_rule "tunm.1" {
  caption "tunm.1 : min. tunm width : 0.41um"
  edge_width TUNM -lt 0.41
}

drc_rule "tunm.2" {
  caption "tunm.2 : min. tunm spacing : 0.5um"
  spacing -same_layer TUNM TUNM -lt 0.5
}

drc_rule "tunm.4" {
  caption "tunm.4 : min. tunm spacing to gate outside tunm: 0.095um"
  spacing -same_layer TUNM TUNM -lt 0.095
}

drc_rule "tunm.5" {
  caption "tunm.5 : gate must not straddle tunm"
  extension TUNM TUNM -eq 0
}

drc_rule "tunm.6a" {
  caption "tunm.6a : tunm not allowed outside dnwell"
  and TUNM DNWELL
}

drc_rule "tunm.7" {
  caption "tunm.7 : min. tunm area : 0.672um²"
  area TUNM -lt 0.672
}

drc_rule "poly.1a" {
  caption "poly.1a : min. poly width : 0.15um"
  edge_width POLY -lt 0.15
}

drc_rule "poly.1b" {
  caption "poly.1b: min. lvtn gate width : 0.35um"
  edge_width LVTN -lt 0.35
}

drc_rule "poly.2" {
  caption "poly.2 : min. poly spacing : 0.21um"
  spacing -same_layer POLY POLY -lt 0.21
}

drc_rule "poly.3" {
  caption "poly.3 : min. poly resistor width : 0.33um"
  edge_width POLY_RS -lt 0.33
}

drc_rule "poly.4" {
  caption "poly.4 : min. poly on field spacing to diff : 0.075um"
  spacing POLY NDIFF -lt 0.075
  spacing POLY PDIFF -lt 0.075
}

drc_rule "poly.5" {
  caption "poly.5 : min. poly on field spacing to tap : 0.055um"
```

```
  spacing POLY TAP -lt 0.055
}

drc_rule "poly.6" {
  caption "poly.6 : min. gate spacing to tap : 0.3um"
  spacing NGATE TAP -lt 0.3
  spacing PGATE TAP -lt 0.3
}

drc_rule "poly.7" {
  caption "poly.7 : min. source/drain length : 0.25um"
  not DIFF POLY -layerOut source
  not DIFF POLY -layerOut drain
  edge_ywidth drain -lt 0.25
  edge_ywidth source -lt 0.25
}

drc_rule "poly.8" {
  caption "poly.8 : min. poly extention gate (endcap) : 0.13um"
  extension PGATE POLY -lt 0.13
  extension NGATE POLY -lt 0.13
}

drc_rule "poly.9" {
  caption "poly.9 : min. poly resistor space to poly or diff/tap : 0.48um"
  spacing POLY POLY_RS -lt 0.48
}

drc_rule "poly.10" {
  caption "poly.10 : poly must not overlap diff corner"
get_corners  DIFF -layerOut CD
and CD POLY
}

drc_rule "poly.12" {
  caption "poly.12 : poly must not overlap tap"
  and POLY TAP
}

drc_rule "poly.15" {
  caption "poly.15 : poly must not overlap diff resistor"
  and POLY DIFF_RS
}

drc_rule "rpm.1a" {
  caption "rpm.1a : min. rpm width : 1.27um"
  edge_width RPM -lt 1.27
}

drc_rule "rpm.2" {
  caption "rpm.2 : min. rpm spacing : 0.84um"
  spacing RPM RPM -lt 0.84
}

drc_rule "rpm.3" {
  caption "rpm.3 : min. rpm enclosure of poly resistor : 0.2um"
  enclosure -all_side POLY_RS POLY -lt 0.2
}

drc_rule "rpm.4" {
  caption "rpm.4 : min. psdm enclosure of poly resistor : 0.11um"
  enclosure -all_side POLY_RS PSDM  -lt 0.11
```

```
}

drc_rule "rpm.5" {
  caption "rpm.5 : min. npc enclosure of poly resistor : 0.095um"
  enclosure -all_side POLY_RS NPC -lt 0.095
}

drc_rule "rpm.6" {
  caption "rpm.6 : min. rpm spacing nsdm: 0.2um"
  spacing RPM NSDM -lt 0.2
}

drc_rule "rpm.7" {
  caption "rpm.7 : min. rpm spacing poly: 0.2um"
  spacing RPM POLY -lt 0.2
}

drc_rule "rpm.8" {
  caption "rpm.8 : poly must not straddle rpm"
  extension RPM POLY -eq 0
}

drc_rule "rpm.9" {
  caption "rpm.9 : min. poly resistor spacing hvntm: 0.185um"
  spacing RPM HVNTM -lt 0.185
}

drc_rule "rpm.10" {
  caption "rpm.107 : min. rpm spacing pwbm: 0.001"
  spacing RPM PWBM -lt 0.001
}

drc_rule "varac.1" {
  caption "varac.1: min. varac channel length : 0.18um"
  edge_length VARAC -lt 0.18
}

drc_rule "varac.2" {
  caption "varac.2: min. varac channel width : 1.0um"
  edge_width VARAC -lt 1.0
}

drc_rule "varac.3" {
  caption "varac.3: min. varac channel space to hvtp : 0.18um"
  spacing VARAC HVTP -lt 0.18
}

drc_rule "varac.4" {
  caption "varac.4: min. varac channel space to licon on tap : 0.25um"
  spacing VARAC LICON -lt 0.25
}

drc_rule "varac.5" {
  caption "varac.5: min. nwell enclosure of poly overlapping varac channel : 0.15um"
  enclosure -all_side VARAC NWELL -lt 0.15
}

drc_rule "varac.6" {
  caption "varac.6: min. varac channel tap space to difftap : 0.27um"
  spacing VARAC DIFFTAP -lt 0.27
}
```

```
drc_rule "varac.7" {
  caption "varac.7:  nwell overlapping varac channel must not overlap p+diff"
  and VARAC NWELL
}

drc_rule "photo.2" {
  caption "photo.2 : minimum/maximum width of photodiode : 3.0um"
  edge_width PHOTO -lt 3.0
}

drc_rule "photo.3" {
  caption "photo.3 : mini. photodiode spacing : 5.0um"
  spacing PHOTO PHOTO -lt 5.0
}

drc_rule "photo.4" {
  caption "photo.4 : mini. photodiode spacing to dnwell : 5.3um"
  spacing PHOTO DNWELL -lt 5.3
}

drc_rule "photo.5.6" {
  caption "photo.5.6 : photodiode edges must coincide areaid.po and enclosed by dnwell"
  not PHOTO DNWELL
}

drc_rule "photo.7" {
  caption "photo.7 : photodiode must be enclosed by p+tap ring"
  not PHOTO PHOTO
}

drc_rule "photo.8" {
  caption "photo.8 : minimum/maximum width of nwell inside photodiode : 0.84um"
  not PHOTO NWELL
}

drc_rule "photo.9" {
  caption "photo.9 : minimum/maximum enclosure of nwell by photodiode : 1.08um"
  enclosure -all_side PHOTO NWELL -lt 1.08
}

drc_rule "photo.10" {
  caption "photo.10 : minimum/maximum width of tap inside photodiode : 0.41um"
  not PHOTO PHOTO
}

drc_rule "npc.1" {
  caption "npc.1 : min. npc width : 0.27um"
  edge_width NPC -lt 0.27
}

drc_rule "npc.2" {
  caption "npc.2 : min. npc spacing, should be mnually merge if less : 0.27um"
  spacing -same_layer NPC NPC -lt 0.27
}

drc_rule "npc.4" {
  caption "npc.4 : min. npc spacing to gate : 0.09um"
  spacing NPC NGATE -lt 0.09
  spacing NPC PGATE -lt 0.09
}

drc_rule "nsdm.1" {
```

```
  caption "nsdm.1 : min. nsdm width : 0.38um"
  edge_width NSDM -lt 0.38
}

drc_rule "psdm.1" {
  caption "psdm.1 : min. psdm width : 0.38um"
  edge_width PSDM -lt 0.38
}

drc_rule "n/psdm.1" {
  caption "n/psdm.1 : min. nsdm spacing, should be mnually merge if less : 0.38um"
  spacing N/PSDM NSDM -lt 0.38
}

drc_rule "n/psdm.1" {
  caption "n/psdm.1 : min. psdm spacing, should be mnually merge if less : 0.38um"
  spacing N/PSDM PSDM -lt 0.38
}

drc_rule "n/psdm.5a" {
  caption "n/psdm.5a : min. n/psdm enclosure diff except butting edge : 0.125um"
  enclosure -all_side N/PSDM PSDM -lt 0.125
}

drc_rule "n/psdm.5b" {
  caption "n/psdm.5b : min. n/psdm enclosure tap except butting edge : 0.125um"
  enclosure -all_side N/PSDM PSDM -lt 0.125
}

drc_rule "n/psdm.6" {
  caption "n/psdm.6 : min. n/psdm enclosure of butting edge : 0.0um"
  enclosure -all_side N/PSDM PSDM -lt 0.0
}

drc_rule "n/psdm.7" {
  caption "n/psdm.7 : min. nsdm diff spacing to psdm diff except butting edge : 0.13um"
  spacing N/PSDM NSDM -lt 0.13
}

drc_rule "tap and diff" {
  caption "tap and diff must not overlap"
  and TAP DIFF
}

drc_rule "n/psdm.10a" {
  caption "n/psdm.10a : min. nsdm area : 0.265um²"
  area N/PSDM -lt 0.265
}

drc_rule "n/psdm.10b" {
  caption "n/psdm.10b : min. psdm area : 0.265um²"
  area N/PSDM -lt 0.265
}

drc_rule "licon.1" {
  caption "licon.1 : minimum/maximum width of licon : 0.17um"
  edge_width LICON -lt 0.17
}

drc_rule "licon.1b/c" {
  caption "licon.1b/c : minimum/maximum width/length of licon inside poly resistor : 2.0/0.19um"
  and LICON POLY_RS -layerOut poly_rs_licon
```

```
  edge_width poly_rs_licon -lt 0.19
}

drc_rule "licon.2" {
  caption "licon.2 : min. licon spacing : 0.17um"
  spacing -same_layer LICON LICON -lt 0.17
}

drc_rule "licon.2b" {
  caption "licon.2b : min. licon 0.19um edge on resistor spacing : 0.35um"
  //edge_width LICON -lt 0.19 -layerOut li19
  //spacing li19 li19 -lt 0.35
  //TODO
}

drc_rule "licon.2c" {
  caption "licon.2c : min. licon 2.0um edge on resistor spacing : 0.51um"
  //edge_width LICON -lt 0.20 -layerOut li20
  //spacing li20 li20 -lt 0.51
  //TODO
}

drc_rule "licon.2d" {
  caption "licon.2d : min. licon on resistor spacing other licon : 0.51um"
  //spacing -same_layer LICON LICON -lt 0.51
  //TODO
}

drc_rule "licon.5" {
  caption "licon.5 : min. diff enclosure of licon : 0.04um"
  get_intersecting LICON DIFF -layerOut diff_licon
  enclosure -all_side diff_licon DIFF -lt 0.04
}

drc_rule "licon.6" {
  caption "licon.6 : min. abutting edge spacing to licon tap : 0.06um"
  spacing LICON LICON -lt 0.06
}

drc_rule "licon.7" {
  caption "licon.7 : min. tap enclosure of licon by one of 2 opposite edges : 0.12um"
  get_intersecting LICON TAP -layerOut tap_licon
  enclosure -opposite_side tap_licon TAP -lt 0.12
}

drc_rule "licon.8" {
  caption "licon.8 : min. poly enclosure of licon : 0.05um"
  get_intersecting LICON POLY -layerOut licon_poly
  enclosure -all_side licon_poly POLY -lt 0.05
}

drc_rule "licon.8a" {
  caption "licon.8a : min. poly enclosure of licon by one of 2 opposite edges : 0.08um"
  enclosure -opposite_side licon_poly POLY -lt 0.08
}

drc_rule "licon.10" {
  caption "licon.10 : min. licon spacing to varac channel : 0.25um"
  spacing LICON VARAC -lt 0.25
}

drc_rule "licon.11" {
```

```
  caption "licon.11 : min. licon spacing to gate : 0.055um"
  spacing LICON LICON -lt 0.055
}

drc_rule "licon.11a" {
  caption "licon.11a : min. licon spacing to gate inside areaid.sc : 0.05um"
  spacing LICON LICON -lt 0.05
}

drc_rule "licon.11c" {
  caption "licon.11c : min. licon spacing to gate for specific cells: 0.04um"
  spacing LICON LICON -lt 0.04
}

drc_rule "licon.12" {
  caption "licon.12 : max. sd width without licon : 5.7um"
  edge_width LICON -gt 5.7
}

drc_rule "licon.13" {
  caption "licon.13 : min. difftap licon spacing to npc : 0.09um"
  spacing LICON DIFFTAP -lt 0.09
}

drc_rule "licon.14" {
  caption "licon.14 : min. poly licon spacing to difftap : 0.19um"
  spacing LICON DIFFTAP -lt 0.19
}

drc_rule "licon.15" {
  caption "licon.15 : min. npc enclosure of poly-licon : 0.1um"
  get_intersecting LICON POLY -layerOut poly_licon
  enclosure -all_side poly_licon NPC -lt 0.1
}

drc_rule "licon.17" {
  caption "licon.17 : tap must not straddle poly"
  and POLY TAP
}

drc_rule "licon.18" {
  caption "licon.18 : npc must enclosed one poly-licon"
  get_intersecting -neg npc poly_licon
}

drc_rule "vpp.1" {
  caption "vpp.1 : min. vpp width : 1.43um"
  edge_width VPP -lt 1.43
}

drc_rule "vpp.3" {
  caption "vpp.3 : vpp must not overlapp poly or diff or tap"
  and VPP POLY
}

drc_rule "vpp.4" {
  caption "vpp.4 : vpp must not straddle nwell"
  extension VPP NWELL -eq 0
}

drc_rule "vpp.4" {
  caption "vpp.4 : vpp must not straddle dnwell"
```

```
  extension VPP DNWELL -eq 0
}

drc_rule "vpp.5" {
  caption "vpp.5 : min. vpp spacing to poly or li or m1 or m2 : 1.5um"
  spacing VPP POLY -lt 1.5
}

drc_rule "vpp.5a" {
  caption "vpp.5a : max. m3 density in vpp : 0.25"
  //max_density
}

drc_rule "vpp.5b" {
  caption "vpp.5b : max. m4 density in vpp : 0.3"
  //max_density
}

drc_rule "vpp.5c" {
  caption "vpp.5c : max. m5 density in vpp : 0.4"
  //max_density
}

drc_rule "vpp.8" {
  caption "vpp.8 : nwell enclosure of vpp : 1.5"
  enclosure -all_side VPP NWELL -lt  1.5
}

drc_rule "vpp.9" {
  caption "vpp.9 : vpp spacing to nwell : 1.5"
  spacing VPP NWELL -lt 1.5
}

drc_rule "vpp.13" {
  caption "vpp.13 : m1 spacing to m1inside vpp : 0.16"
  spacing VPP MET1 -lt 0.16
}

drc_rule "capm.1" {
  caption "capm.1 : min. capm width : 1.0um"
  edge_width CAPM -lt 1.0
}

drc_rule "capm.2a" {
  caption "capm.2a : min. capm spacing : 0.84um"
  spacing CAPM CAPM -lt 0.84
}

drc_rule "capm.2b" {
  caption "capm.2b : min. capm spacing : 1.2um"
  spacing CAPM CAPM -lt 1.2
}

drc_rule "capm.3" {
  caption "capm.3 : min. m2 enclosure of capm : 0.14um"
  enclosure -all_side CAPM MET2 -lt 0.14
}

drc_rule "capm.4" {
  caption "capm.4 : min. capm enclosure of via2 : 0.14um"
  enclosure -all_side CAPM VIA2 -lt 0.14
}
```

```
drc_rule "capm.5" {
  caption "capm.5 : min. capm spacing to via2 : 0.14um"
  spacing CAPM VIA2 -lt 0.14
}

drc_rule "capm.6" {
  caption "capm.6 : max. capm lenght/width : 20um"
  edge_width CAPM -lt 20
}

drc_rule "capm.8" {
  caption "capm.8 : min. capm spacing to via : 0.14um"
  spacing CAPM VIA -lt 0.14
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle nwell"
  extension CAPM NWELL -eq 0
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle diff"
  extension CAPM CAPM -eq 0
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle tap"
  extension CAPM CAPM -eq 0
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle poly"
  extension CAPM POLY -eq 0
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle li"
  extension CAPM LI -eq 0
}

drc_rule "capm.10" {
  caption "capm.10 : capm must not straddle m1"
  extension CAPM MET1 -eq 0
}

drc_rule "capm.11" {
  caption "capm.11 : min. capm spacing to m2 not overlapping capm : 0.5um"
  spacing CAPM MET2 -lt 0.5
}

drc_rule "li.1" {
  caption "li.1 : min. li width : 0.17um"
  edge_width LI -lt 0.17
}

drc_rule "li.1a" {
  caption "li.1a : min. li width for the cells s8rf2_xcmvpp_hd5_* : 0.14um"
  edge_width LI -lt 0.14
}

drc_rule "li.3" {
```

```
    caption "li.3 : min. li spacing : 0.17um"
    spacing -same_layer LI LI -lt 0.17
  }

  drc_rule "li.3a" {
    caption "li.3a : min. li spacing for the cells s8rf2_xcmvpp_hd5_* : 0.14um"
    //spacing LI LI -lt 0.14
// TODO
  }

  drc_rule "li.5" {
    caption "li.5 : min. li enclosure of licon of 2 opposite edges : 0.08um"
    get_intersecting LICON LI -layerOut li_licon
    enclosure -opposite_side li_licon LI -lt 0.08
  }

  drc_rule "li.6" {
    caption "li.6 : min. li area : 0.0561um²"
    area LI -lt 0.0561
  }

  drc_rule "ct.1" {
    caption "ct.1 : minimum/maximum width of mcon : 0.17um"
    edge_width CT -lt 0.17
  }

  drc_rule "ct.2" {
    caption "ct.2 : min. mcon spacing : 0.19um"
    spacing CT CT -lt 0.19
  }

  drc_rule "ct.4" {
    caption "ct.4 : mcon should covered by li"
    not CT LI
  }

  drc_rule "ct.irdrop.1" {
    caption "ct.irdrop.1 : min. li enclosure of 1..10 mcon : 0.2um"
    //get_intersecting MCON LI -layerOut li_mcon
    //enclosure -all_side li_mcon LI -lt 0.2
    //TODO
  }

  drc_rule "ct.irdrop.2" {
    caption "ct.irdrop.2 : min. li enclosure of 11..100 mcon : 0.3um"
    //enclosure -all_side MCON LI -lt 0.3
    //TODO
  }

  drc_rule "m1.1" {
    caption "m1.1 : min. m1 width : 0.14um"
    edge_width MET1 -lt 14
    //edge_width MET1 -lt 0.14
  }

  drc_rule "m1.2" {
    caption "m1.2 : min. m1 spacing : 0.14um"
    spacing -same_layer MET1 MET1 -lt 14
    //spacing -same_layer MET1 MET1 -lt 0.14
  }

  drc_rule "m1.3ab" {
```

```
  caption "m1.3ab : min. 3um.m1 spacing m1 : 0.28um"
  //spacing MET1 MET1 -lt 3
}

drc_rule "m1.4" {
  caption "m1.4 : min. m1 enclosure of mcon : 0.03um"
  enclosure -all_side MCON MET1 -lt 0.03
}

drc_rule "m1.4a" {
  caption "m1.4a : min. m1 enclosure of mcon for specific cells : 0.005um"
  enclosure -all_side MCON MET1 -lt 0.005
}

drc_rule "m1.6" {
  caption "m1.6 : min. m1 area : 0.083um^2"
  area MET1 -lt 0.083
}

drc_rule "m1.7" {
  caption "m1.7 : min. m1 holes area : 0.14um^2"
  //holes_area MET1 -eq 1
  //TODO
}

drc_rule "m1.5" {
  caption "m1.5 : min. m1 enclosure of mcon of 2 opposite edges : 0.06um"
  enclosure -opposite_side MCON MET1 -lt 0.06
}

drc_rule "m1.11" {
  caption "m1.11 : max. m1 width after slotting : 4.0um"
  edge_width MET1 -gt 4.0
}

drc_rule "via.4c.5c" {
  caption "via.4c.5c : m1 must enclose all via"
  not VIA MET1
}

drc_rule "via.1a" {
  caption "via.1a : minimum/maximum width of via : 0.15um"
  edge_width VIA -lt 0.15
}

drc_rule "via.1b" {
  caption "via.1b : minimum/maximum width of via in areaid.mt: 0.15um or 0.23um or 0.28um"
  edge_width VIA -lt 0.15
}

drc_rule "via.2" {
  caption "via.2 : min. via spacing : 0.17um"
  spacing -same_layer VIA VIA -lt 0.17
}

drc_rule "via.4a" {
  caption "via.4a : min. m1 enclosure of 0.15um via : 0.055um"
  enclosure -all_side VIA MET1 -lt 0.15
}

drc_rule "via.4b" {
  caption "via.4b : min. m1 enclosure of 0.23um via : 0.03um"
```

```
    enclosure -all_side VIA MET1 -lt 0.23
  }

  drc_rule "via1.5a" {
    caption "via1.5a : min. m1 enclosure of 0.15um via of 2 opposite edges : 0.085um"
    enclosure -opposite_side VIA1 MET1 -lt 0.15
  }

  drc_rule "via1.5b" {
    caption "via1.5b : min. m1 enclosure of 0.23um via of 2 opposite edges : 0.06um"
    enclosure -opposite_side VIA1 MET1 -lt 0.23
  }

  drc_rule "via.11" {
    caption "via.11 : minimum/maximum width of via : 0.18um"
    edge_width VIA -lt 0.18
  }

  drc_rule "via.12" {
    caption "via.12 : min. via spacing : 0.13um"
    spacing -same_layer VIA VIA -lt 0.13
  }

  drc_rule "via1.14" {
    caption "via1.14 : min. m1 enclosure of 0.04um via of 2 opposite edges : 0.04um"
    enclosure -opposite_side VIA1 MET1 -lt 0.04
  }

  drc_rule "m2.1" {
    caption "m2.1 : min. m2 width : 0.14um"
    edge_width MET2 -lt 0.14
  }

  drc_rule "m2.2" {
    caption "m2.2 : min. m2 spacing : 0.14um"
    spacing -same_layer MET2 MET2 -lt 0.14
  }

  drc_rule "m2.3ab" {
    caption "m2.3ab : min. 3um.m2 spacing m2 : 0.28um"
    //spacing -same_layer MET2 MET2 -lt 0.28
    //TODO:
  }

  drc_rule "m2.6" {
    caption "m2.6 : min. m2 area : 0.0676um²"
    area MET2 -lt 0.0676
  }

  drc_rule "m2.7" {
    caption "m2.7 : min. m2 holes area : 0.14um²"
    //holes_area MET2 -eq 1
//TODO
  }

  drc_rule "m2.4" {
    caption "m2.4 : min. m2 enclosure of via : 0.055um"
    enclosure -all_side VIA MET2 -lt 0.055
  }

  drc_rule "m2.5" {
    caption "m2.5 : min. m2 enclosure of via of 2 opposite edges : 0.085um"
```

```
  enclosure -opposite_side VIA MET2 -lt 0.085
}

drc_rule "m2.11" {
  caption "m2.11 : max. m2 width after slotting : 4.0um"
  edge_width MET2 -gt 4.0
}

drc_rule "via2" {
  caption "via2 : m2 must enclose all via2"
  not VIA2 MET2
}

drc_rule "via2.1a" {
  caption "via2.1a : minimum/maximum width of via2 : 0.2um"
  edge_width VIA2 -lt 0.2
}

drc_rule "via2.1b" {
  caption "via2.1b : minimum/maximum width of via2 in areaid.mt: 0.2um or 1.2um or 1.5um"
  edge_width VIA2 -lt 0.2
}

drc_rule "via2.2" {
  caption "via2.2 : min. via2 spacing : 0.2um"
  spacing -same_layer VIA2 VIA2 -lt 0.2
}

drc_rule "via2.4" {
  caption "via2.4 : min. m2 enclosure of via2 : 0.04um"
  enclosure -all_side VIA2 MET2 -lt 0.04
}

drc_rule "via2.4a" {
  caption "via2.4a : min. m2 enclosure of 1.5um via2 : 0.14um"
  //enclosure -all_side VIA2 MET2 -lt 1.5
  //TODO
}

drc_rule "via2.5" {
  caption "via2.5 : min. m2 enclosure of via2 of 2 opposite edges : 0.085um"
  enclosure -opposite_side VIA2 MET2 -lt 0.085
}

drc_rule "via2.11" {
  caption "via2.11 : minimum/maximum width of via2 : 0.21um"
  edge_width VIA2 -lt 0.20
}

drc_rule "via2.12" {
  caption "via2.12 : min. via2 spacing : 0.18um"
  spacing -same_layer VIA2 VIA2 -lt 0.18
}

drc_rule "via2.14" {
  caption "via2.14 : min. m2 enclosure of via2 : 0.035um"
  enclosure -all_side VIA2 MET2 -lt 0.035
}

drc_rule "m3.1" {
  caption "m3.1 : min. m3 width : 0.3um"
  edge_width MET3 -lt 0.3
```

```
  }

  drc_rule "m3.2" {
    caption "m3.2 : min. m3 spacing : 0.3um"
    spacing -same_layer MET3 MET3 -lt 0.3
  }

  drc_rule "m3.3ab" {
    caption "m3.3ab : min. 3um.m3 spacing m3 : 0.4um"
    //spacing -same_layer MET3 MET3 -lt 0.4
    //TODO
  }

  drc_rule "m3.6" {
    caption "m3.6 : min. m3 area : 0.24um²"
    area MET3 -lt 0.24
  }

  drc_rule "m3.4" {
    caption "m3.4 : min. m3 enclosure of via2 : 0.065um"
    enclosure -all_side VIA2 MET3 -lt 0.065
  }

  drc_rule "m3.5" {
    caption "m3.5 : min. m3 enclosure of via2 of 2 opposite edges : 0.085um"
    enclosure -opposite_side VIA2 MET3 -lt 0.065
  }

  drc_rule "m3.7" {
    caption "m3.7 : min. m3 holes area : 0.2um²"
    //holes_area MET3 -eq 1
//TODO
  }

  drc_rule "m3.11" {
    caption "m3.11 : max. m3 width after slotting : 4.0um"
    edge_width MET3 -gt 4.0
  }

  drc_rule "via3" {
    caption "via3 : m3 must enclose all via3"
    not VIA3 MET3
  }

  drc_rule "via3.1a" {
    caption "via3.1a : minimum/maximum width of via3 : 0.2um"
    edge_width VIA3 -lt 0.2
  }

  drc_rule "via3.1a" {
    caption "via3.1a : minimum/maximum width of via3 in areaid.mt: 0.2um or 0.8um"
    edge_width VIA3 -lt 0.2
  }

  drc_rule "via3.2" {
    caption "via3.2 : min. via3 spacing : 0.2um"
    spacing VIA3 VIA3 -lt 0.2
  }

  drc_rule "via3.4" {
    caption "via3.4 : min. m3 enclosure of via3 : 0.06um"
    enclosure -all_side VIA3 MET3 -lt 0.06
```

```
  }

  drc_rule "via3.5" {
    caption "via3.5 : min. m2 enclosure of via3 of 2 opposite edges : 0.09um"
    enclosure -opposite_side VIA3 MET3 -lt 0.09
  }

  drc_rule "via3.11" {
    caption "via3.11 : minimum/maximum width of via3 : 0.21um"
    edge_width VIA3 -lt 0.20
  }

  drc_rule "via3.12" {
    caption "via3.12 : min. via3 spacing : 0.18um"
    spacing VIA3 VIA3 -lt 0.18
  }

  drc_rule "via3.13" {
    caption "via3.13 : min. m3 enclosure of via3 : 0.055um"
    enclosure -all_side VIA3 MET3 -lt 0.055
  }

  drc_rule "m4.1" {
    caption "m4.1 : min. m4 width : 0.3um"
    edge_width MET4 -lt 0.3
  }

  drc_rule "m4.2" {
    caption "m4.2 : min. m4 spacing : 0.3um"
    spacing -same_layer MET4 MET4 -lt 0.3
  }

  drc_rule "m4.5ab" {
    caption "m4.5ab : min. 3um.m4 spacing m4 : 0.4um"
    spacing MET4 MET4 -lt 3
  }

  drc_rule "m4.4" {
    caption "m4.4 : min. m4 area : 0.24um²"
    area MET4 -lt 0.24
  }

  drc_rule "m4.3" {
    caption "m4.3 : min. m4 enclosure of via3 : 0.065um"
    enclosure -all_side VIA3 MET4 -lt 0.065
  }

  drc_rule "m4.5" {
    caption "m4.5 : min. m4 enclosure of via3 of 2 opposite edges : 0.085um"
    enclosure -opposite_side VIA3 MET4 -lt 0.085
  }

  drc_rule "m4.7" {
    caption "m4.7 : min. m4 holes area : 0.2um²"
    //holes_area MET4 -eq 1
//TODO
  }

  drc_rule "m4.11" {
    caption "m4.11 : max. m4 width after slotting : 10.0um"
    edge_width MET4 -gt 10.0
  }
```

```
drc_rule "m4.15" {
  caption "m4.15 : min. m4 enclosure of via3 : 0.06um"
  enclosure -all_side VIA3 MET4 -lt 0.06
}

drc_rule "via4.1a" {
  caption "via4.1a : minimum/maximum width of via4 : 0.8um"
  edge_width VIA4 -lt 0.8
}

drc_rule "via4.2" {
  caption "via4.2 : min. via4 spacing : 0.8um"
  spacing -same_layer VIA4 VIA4 -lt 0.8
}

drc_rule "via4.4" {
  caption "via4.4 : min. m4 enclosure of via4 : 0.19um"
  enclosure -all_side VIA4 MET4 -lt 0.19
}

drc_rule "via4" {
  caption "via4 : m4 must enclose all via4"
  not VIA4 MET4
}

drc_rule "m5.1" {
  caption "m5.1 : min. m5 width : 1.6um"
  edge_width MET5 -lt 1.6
}

drc_rule "m5.2" {
  caption "m5.2 : min. m5 spacing : 1.6um"
  spacing -same_layer MET5 MET5 -lt 1.6
}

drc_rule "m5.3" {
  caption "m4.3 : min. m5 enclosure of via4 : 0.31um"
  enclosure -all_side VIA4 MET5 -lt 0.31
}

drc_rule "nsm.1" {
  caption "nsm.1 : min. nsm width : 3.0um"
  edge_width NSM -lt 3.0
}

drc_rule "nsm.2" {
  caption "nsm.2 : min. nsm spacing : 4.0um"
  spacing -same_layer NSM NSM -lt 4.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of diff : 3.0um"
  enclosure -all_side DIFF NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of tap : 3.0um"
  enclosure -all_side TAP NSM -lt 3.0
}

drc_rule "nsm.4" {
```

```
  caption "nsm.4 : min. nsm enclosure of poly : 3.0um"
  enclosure -all_side POLY NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of li : 3.0um"
  enclosure -all_side LI NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of m1 : 3.0um"
  enclosure -all_side MET1 NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of m2 : 3.0um"
  enclosure -all_side MET2 NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of m3 : 3.0um"
  enclosure -all_side MET3 NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of m4 : 3.0um"
  enclosure -all_side MET4 NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of m5 : 3.0um"
  enclosure -all_side MET5 NSM -lt 3.0
}

drc_rule "nsm.4" {
  caption "nsm.4 : min. nsm enclosure of cfom : 3.0um"
  enclosure -all_side CFOM NSM -lt 3.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to diff : 1.0um"
  spacing NSM DIFF -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to tap : 1.0um"
  spacing NSM TAP -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to poly : 1.0um"
  spacing NSM POLY -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to li : 1.0um"
  spacing NSM LI -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to m1 : 1.0um"
  spacing NSM MET1 -lt 1.0
```

```
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to m2 : 1.0um"
  spacing NSM MET2 -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to m3 : 1.0um"
  spacing NSM MET3 -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to m4 : 1.0um"
  spacing NSM MET4 -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to m5 : 1.0um"
  spacing NSM MET5 -lt 1.0
}

drc_rule "nsm.3" {
  caption "nsm.3 : min. nsm spacing to cfom : 1.0um"
  spacing NSM NSM -lt 1.0
}

drc_rule "pad.2" {
  caption "pad.2 : min. pad spacing : 1.27um"
  spacing -same_layer PAD PAD -lt 1.27
}

drc_rule "mf.1" {
  caption "mf.1 : minimum/maximum width of fuse : 0.8um"
  edge_width MF -lt 0.8
}

drc_rule "mf.2" {
  caption "mf.2 : minimum/maximum length of fuse : 7.2um"
  edge_length MF -lt 7.2
}

drc_rule "mf.3" {
  caption "mf.3 : min. fuse center spacing : 2.76um"
  spacing MF MF -lt 2.76
}

drc_rule "hvi.1" {
  caption "hvi.1 : min. hvi width : 0.6um"
  edge_width HVI -lt 0.6
}

drc_rule "hvi.2" {
  caption "hvi.2 : min. hvi spacing, merge if less : 0.7um"
  spacing -same_layer HVI HVI -lt 0.7
}

drc_rule "hvi.4" {
  caption "hvi.4 : hvi must not overlapp tunm"
  and HVI TUNM
}
```

```
drc_rule "hvnwell.8" {
  caption "hvnwelli.8 : min. hvnwel spacing to nwell : 2.0"
  spacing HVNWELL NWELL -lt 2
}

drc_rule "hvdifftap.14" {
  caption "hvdifftap.14 : min. diff inside hvi width : 0.29um"
  not HVDIFFTAP HVI
}

drc_rule "hvdifftap.14a" {
  caption "hvdifftap.14a : min. p+diff resistor inside hvi width : 0.15um"
  not HVDIFFTAP HVI
}

drc_rule "hvdifftap.15a" {
  caption "hvdifftap.15a : min. diff inside hvi spacing : 0.3um"
  spacing HVDIFFTAP HVI -lt 0.3
}

drc_rule "hvdifftap.15b" {
  caption "hvdifftap.15b : min. n+diff inside hvi spacing to p+diff inside hvi except abutting: 0.37um"
  spacing HVDIFFTAP HVI -lt 0.37
}

drc_rule "hvdifftap.16" {
  caption "hvdifftap.16 : min. tap inside hvi abuttng diff : 0.7um"
  not HVDIFFTAP HVI
}

drc_rule "hvdifftap.17" {
  caption "hvdifftap.17 : min. hvnwell enclosure of p+diff : 0.33um"
  enclosure -all_side HVDIFFTAP HVNWELL -lt 0.33
}

drc_rule "hvdifftap.18" {
  caption "hvdifftap.18 : min. hvnwell spacing to n+diff : 0.43um"
  spacing HVDIFFTAP HVNWELL -lt 0.43
}

drc_rule "hvdifftap.19" {
  caption "hvdifftap.19 : min. hvnwell enclosure of n+tap : 0.33um"
  enclosure -all_side HVDIFFTAP HVNWELL -lt 0.33
}

drc_rule "hvdifftap.20" {
  caption "hvdifftap.20 : min. hvnwell spacing to p+tap : 0.43um"
  spacing HVDIFFTAP HVNWELL -lt 0.43
}

drc_rule "hvdifftap.21" {
  caption "hvdifftap.21 : diff must not straddle hvi"
  extension HVDIFFTAP HVI -eq 0
}

drc_rule "hvdifftap.21" {
  caption "hvdifftap.21 : tap must not straddle hvi"
  extension HVDIFFTAP HVI -eq 0
}

drc_rule "hvdifftap.22" {
  caption "hvdifftap.22 : min. hvi enclosure of diff or tap : 0.18um"
```

```
  enclosure -all_side HVDIFFTAP HVI -lt 0.18
}

drc_rule "hvdifftap.23" {
  caption "hvdifftap.23 : min. hvi spacing to diff or tap : 0.18um"
  spacing HVDIFFTAP HVI -lt 0.18
}

drc_rule "hvdifftap.24" {
  caption "hvdifftap.24 : min. hv n+diff spacing to nwell : 0.43um"
  spacing HVDIFFTAP NWELL -lt 0.43
}

drc_rule "hvdifftap.25" {
  caption "hvdifftap.25 : min. n+diff inside hvi spacing accros p+tap  : 1.07um"
  spacing HVDIFFTAP HVI -lt 1.07
}

drc_rule "hvpoly.13" {
  caption "hvpoly.13: min. hvi gate length : 0.5um"
  edge_length HVPOLY -lt 0.5
}

drc_rule "hvpoly.14" {
  caption "hvpoly.14 : poly must not straddle hvi"
  extension HVPOLY POLY -eq 0
}

drc_rule "hvntm.1" {
  caption "hvntm.1 : min. hvntm width : 0.7um"
  edge_width HVNTM -lt 0.7
}

drc_rule "hvntm.2" {
  caption "hvntm.2 : min. hvntm spacing : 0.7um"
  spacing HVNTM HVNTM -lt 0.7
}

drc_rule "hvntm.3" {
  caption "hvntm.3 : min. hvntm enclosure of hv n+diff : 0.185um"
  enclosure -all_side HVNTM HV -lt 0.185
}

drc_rule "hvntm.4" {
  caption "hvntm.4 : min. hvntm spacing to n+diff : 0.185um"
  spacing HVNTM HVNTM -lt 0.185
}

drc_rule "hvntm.5" {
  caption "hvntm.5 : min. hvntm spacing to p+diff : 0.185um"
  spacing HVNTM HVNTM -lt 0.185
}

drc_rule "hvntm.6a" {
  caption "hvntm.6a : min. hvntm spacing to p+tap : 0.185um"
  spacing HVNTM HVNTM -lt 0.185
}

drc_rule "hvntm.9" {
  caption "hvntm.9 : hvntm must not overlapp areaid.ce"
  and HVNTM HVNTM
}
```

```
drc_rule "denmos.1" {
  caption "denmos.1 : min. de_nfet gate width : 1.055um"
  edge_width DENMOS -lt 1.055
}

drc_rule "denmos.2" {
  caption "denmos.2 : min. de_nfet source ouside poly width : 0.28um"
  edge_width DENMOS -lt 0.28
}

drc_rule "denmos.3" {
  caption "denmos.3 : min. de_nfet source inside poly width : 0.925um"
  not DENMOS POLY
}

drc_rule "denmos.4" {
  caption "denmos.4 : min. de_nfet drain width : 0.17um"
  edge_width DENMOS -lt 0.17
}

drc_rule "denmos.5" {
  caption "denmos.5 : min. de_nfet source inside nwell width : 0.225m"
  not DENMOS NWELL
}

drc_rule "denmos.6" {
  caption "denmos.6 : min. de_nfet source spacing to drain : 1.585um"
  spacing DENMOS DENMOS -lt 1.585
}

drc_rule "denmos.7" {
  caption "denmos.7 : min. de_nfet channel width : 5.0um"
  edge_width DENMOS -lt 5.0
}

drc_rule "denmos.10" {
  caption "denmos.10 : min. nwell enclosure of de_nfet drain : 0.66um"
  enclosure -all_side DENMOS NWELL -lt 0.66
}

drc_rule "denmos.11" {
  caption "denmos.11 : min. de_nfet nwell spacing to tap : 0.86um"
  spacing DENMOS NWELL -lt 0.86
}

drc_rule "denmos.13" {
  caption "denmos.13 : min. nsdm enclosure of de_nfet source : 0.13um"
  enclosure -all_side DENMOS NSDM -lt 0.13
}

drc_rule "depmos.1" {
  caption "depmos.1 : min. de_pfet gate width : 1.05um"
  edge_width DEPMOS -lt 1.05
}

drc_rule "depmos.2" {
  caption "depmos.2 : min. de_pfet source ouside poly width : 0.28um"
  edge_width DEPMOS -lt 0.28
}

drc_rule "depmos.3" {
```

```
  caption "depmos.3 : min. de_pfet source inside poly width : 0.92um"
  not DEPMOS POLY
}

drc_rule "depmos.4" {
  caption "depmos.4 : min. de_pfet drain width : 0.17um"
  edge_width DEPMOS -lt 0.17
}

drc_rule "depmos.5" {
  caption "depmos.5 : min. de_pfet source inside nwell width : 0.26m"
  not DEPMOS NWELL
}

drc_rule "depmos.6" {
  caption "depmos.6 : min. de_pfet source spacing to drain : 1.19um"
  spacing DEPMOS DEPMOS -lt 1.19
}

drc_rule "depmos.7" {
  caption "depmos.7 : min. de_pfet channel width : 5.0um"
  edge_width DEPMOS -lt 5.0
}

drc_rule "depmos.10" {
  caption "depmos.10 : min. pwell enclosure of de_pfet drain : 0.86um"
  enclosure -all_side DEPMOS DEPMOS -lt 0.86
}

drc_rule "depmos.11" {
  caption "depmos.11 : min. de_pfet pwell spacing to tap : 0.66um"
  spacing DEPMOS DEPMOS -lt 0.66
}

drc_rule "depmos.12" {
  caption "depmos.12 : min. psdm enclosure of de_pfet source : 0.13um"
  enclosure -all_side DEPMOS PSDM -lt 0.13
}

drc_rule "extd.1" {
  caption "extd.1 : difftap must not straddle areaid.en"
  extension EXTD DIFFTAP -eq 0
}

drc_rule "extd.2" {
  caption "extd.2 : poly must not overlapp entirely difftap in areaid.en"
  and EXTD DIFFTAP
}

drc_rule "vhvi.1" {
  caption "vhvi.1 : min. vhvi width : 0.02um"
  edge_width VHVI -lt 0.02
}

drc_rule "vhvi.2" {
  caption "vhvi.2 : vhvi must not overlap areaid.ce"
  and VHVI VHVI
}

drc_rule "vhvi.3" {
  caption "vhvi.3 : vhvi must not overlap hvi"
  and VHVI HVI
```

```
}

drc_rule "vhvi.5" {
  caption "vhvi.5 : vhvi must not straddle diff"
  extension VHVI VHVI -eq 0
}

drc_rule "vhvi.5" {
  caption "vhvi.5 : vhvi must not straddle tap"
  extension VHVI VHVI -eq 0
}

drc_rule "vhvi.7" {
  caption "vhvi.7 : vhvi must not straddle poly"
  extension VHVI POLY -eq 0
}

drc_rule "hv.nwell.1" {
  caption "hv.nwell.1 : min. vhvi nwell spacing to nwell : 2.5um"
  spacing HV NWELL -lt 2.5
}

drc_rule "hv.diff.1" {
  caption "hv.diff.1 : min. vhvi diff spacing : 0.3um"
  spacing HV VHVI -lt 0.3
}

drc_rule "hv.diff.2" {
  caption "hv.diff.2 : min. vhvi nwell spacing n+diff : 0.43um"
  spacing HV NWELL -lt 0.43
}

drc_rule "hv.diff.3a" {
  caption "hv.diff.3a : min. vhvi n+diff spacing nwell : 0.55um"
  spacing HV NWELL -lt 0.55
}

drc_rule "hv.poly.2" {
  caption "hv.poly.2 : min. vhvi poly spacing to diff : 0.3um"
  spacing HV POLY -lt 0.3
}

drc_rule "hv.poly.3" {
  caption "hv.poly.3 : min. vhvi poly spacing to nwell : 0.55um"
  spacing HV NWELL -lt 0.55
}

drc_rule "hv.poly.4" {
  caption "hv.poly.4 : min. nwell enclosure of vhvi poly : 0.3um"
  enclosure -all_side VHVI NWELL -lt 0.3
}

drc_rule "hv.poly.6" {
  caption "hv.poly.6 : min. poly enclosure of hvfet gate : 0.16um"
  enclosure -all_side HV POLY -lt 0.16
}

drc_rule "uhvi.1" {
  caption "uhvi.1 : diff must not straddle uhvi"
  extension UHVI UHVI -eq 0
}
```

```
drc_rule "uhvi.1" {
  caption "uhvi.1 : tap must not straddle uhvi"
  extension UHVI UHVI -eq 0
}

drc_rule "uhvi.2" {
  caption "uhvi.2 : poly must not straddle uhvi"
  extension UHVI POLY -eq 0
}

drc_rule "uhvi.3" {
  caption "uhvi.3 : uhvi must not enclose pwbm"
  and UHVI PWBM
}

drc_rule "uhvi.4" {
  caption "uhvi.4 : dnwell must not straddle uhvi"
  extension UHVI DNWELL -eq 0
}

drc_rule "uhvi.5" {
  caption "uhvi.5 : uhvi must not enclose areaid.en20"
  and UHVI UHVI
}

drc_rule "uhvi.6" {
  caption "uhvi.6 : uhvi must not enclose dnwell"
  and UHVI DNWELL
}

drc_rule "uhvi.7" {
  caption "uhvi.7 : uhvi must not enclose natfet"
  and UHVI UHVI
}

drc_rule "pwres.2" {
  caption "pwres.2 : min. pwell resistor width : 2.65um"
  edge_width PWRES -lt 2.65
}

drc_rule "pwres.2" {
  caption "pwres.2 : max. pwell resistor width : 2.65um"
  edge_width PWRES -lt 2.65
}

drc_rule "pwres.3" {
  caption "pwres.3 : min. pwell resistor length : 26.5um"
  edge_length PWRES -lt 26.5
}

drc_rule "pwres.4" {
  caption "pwres.4 : max. pwell resistor length : 265um"
  edge_length PWRES -lt 265
}

drc_rule "pwres.5" {
  caption "pwres.5 : min. pwell resistor tap spacing to nwell : 0.22um"
  spacing PWRES NWELL -lt 0.22
}

drc_rule "pwres.5" {
  caption "pwres.5 : max. pwell resistor tap spacing to nwell : 0.22um"
```

```
  spacing PWRES NWELL -lt 0.22
}

drc_rule "pwres.6" {
  caption "pwres.6 : min. width of tap inside pwell resistor : 0.53um"
  not PWRES PWRES
}

drc_rule "pwres.6" {
  caption "pwres.6 : max. width of tap inside pwell resistor : 0.53um"
  not PWRES PWRES
}

drc_rule "pwres.8" {
  caption "pwres.8 : diff not allowed inside pwell resistor"
  not PWRES PWRES
}

drc_rule "pwres.8" {
  caption "pwres.8 : poly not allowed inside pwell resistor"
  not PWRES POLY
}

drc_rule "rfdiode.1" {
  caption "rfdiode.1 : non 90 degree angle areaid.re"
  //area RFDIODE -lt ?
  //TODO:
}

drc_rule "rfdiode.2" {
  caption "rfdiode.2 : areaid.re must coincide rf nwell diode"
  //area RFDIODE -lt ?
  //TODO:
}

drc_rule "areaid_re_OFFGRID" {
  caption "x.1b : OFFGRID vertex on areaid.re"
  //area AREAID_RE_OFFGRID -lt ?
  //TODO:
}


// "capm.7 : capm not rectangle"
// "ct.irdrop.1 : min. li enclsoure of 1..10 mcon : 0.2um"
// "ct.irdrop.2 : min. li enclsoure of 11..100 mcon : 0.3um"
// "denmos.12 : min. de_nfet nwell : 2.4um"
// "denmos.8 : 90deg. not allowed for de_nfet drain"
// "denmos.9a : 45deg. bevels of de_nfet nwell should be 0.43um from corners"
// "denmos.9a : 90deg. not allowed for de_nfet nwell"
// "denmos.9b : 45deg. bevels of de_nfet drain should be 0.05um from corners"
// "depmos.8 : 90deg. not allowed for de_pfet drain"
// "depmos.9a : 45deg. bevels of de_pfet pwell should be 0.43um from corners"
// "depmos.9a : 90deg. not allowed for de_pfet pwell"
// "depmos.9b : 45deg. bevels of de_pfet drain should be 0.05um from corners"
// "difftap.4 : min. tap bound by diffusion : 0.29um"
// "difftap.5 : min. tap bound by 2 diffusions : 0.4um"
// "difftap.6 : diff and tap not allowed to extend beyong their abutting ege"
// "hvnwell.9 : hvi must overlapp hvnwell"
// "licon.16 : diff must enclose one licon"
// "licon.16 : tap must enclose one licon"
// "licon.4 : min. licon must overlap li and (poly or tap or diff) "
// "m2.via : m2 must enclose via"
```

```
// "m3.via2 : m3 must enclose via2"
// "m4.via3 : m4 must enclose via3"
// "m5.via4 : m5 must enclose via4"
// "n/psdm.8 : diff should be the opposite type of well/substrate underneath"
// "n/psdm.8 : tap should be the same type of well/substrate underneath"
// "nwell.7 : min. dnwell separation nwell : 4.5um"
// "poly.11 : non 90 degree angle gate"
// "tunm.3 : min. tunm beyond gate : 0.095um"
// "varac.2: min. varac channel wdth : 1.0um"
// "x.1b : OFFGRID vertex on diff"
// "x.1b : OFFGRID vertex on dnwell"
// "x.1b : OFFGRID vertex on hvi"
// "x.1b : OFFGRID vertex on hvntm"
// "x.1b : OFFGRID vertex on hvtp"
// "x.1b : OFFGRID vertex on hvtr"
// "x.1b : OFFGRID vertex on li"
// "x.1b : OFFGRID vertex on licon"
// "x.1b : OFFGRID vertex on lvtn"
// "x.1b : OFFGRID vertex on m1"
// "x.1b : OFFGRID vertex on m2"
// "x.1b : OFFGRID vertex on m3"
// "x.1b : OFFGRID vertex on m4"
// "x.1b : OFFGRID vertex on m5"
// "x.1b : OFFGRID vertex on mcon"
// "x.1b : OFFGRID vertex on mf"
// "x.1b : OFFGRID vertex on ncm"
// "x.1b : OFFGRID vertex on npc"
// "x.1b : OFFGRID vertex on nsdm"
// "x.1b : OFFGRID vertex on nsm"
// "x.1b : OFFGRID vertex on nwell"
// "x.1b : OFFGRID vertex on pad"
// "x.1b : OFFGRID vertex on poly"
// "x.1b : OFFGRID vertex on psdm"
// "x.1b : OFFGRID vertex on pwbm"
// "x.1b : OFFGRID vertex on pwde"
// "x.1b : OFFGRID vertex on pwell_rs"
// "x.1b : OFFGRID vertex on rpm"
// "x.1b : OFFGRID vertex on tap"
// "x.1b : OFFGRID vertex on tunm"
// "x.1b : OFFGRID vertex on uhvi"
// "x.1b : OFFGRID vertex on vhvi"
// "x.1b : OFFGRID vertex on via"
// "x.1b : OFFGRID vertex on via2"
// "x.1b : OFFGRID vertex on via3"
// "x.1b : OFFGRID vertex on via4"
// "x.1b : OFFGRID vertex on vpp"
// "x.2 : non 90 degree angle diff"
// "x.2 : non 90 degree angle licon"
// "x.2 : non 90 degree angle mcon"
// "x.2 : non 90 degree angle mf"
// "x.2 : non 90 degree angle poly"
// "x.2 : non 90 degree angle tap"
// "x.2 : non 90 degree angle via"
// "x.2 : non 90 degree angle via2"
// "x.2 : non 90 degree angle via3"
// "x.2 : non 90 degree angle via4"
// "x.2c : non 45 degree angle diff"
// "x.2c : non 45 degree angle tap"
// "x.3a : non 45 degree angle dnwell"
// "x.3a : non 45 degree angle hvi"
// "x.3a : non 45 degree angle hvntm"
// "x.3a : non 45 degree angle hvtp"
```

```
 // "x.3a : non 45 degree angle hvtr"
 // "x.3a : non 45 degree angle li"
 // "x.3a : non 45 degree angle lvtn"
 // "x.3a : non 45 degree angle m1"
 // "x.3a : non 45 degree angle m2"
 // "x.3a : non 45 degree angle m3"
 // "x.3a : non 45 degree angle m4"
 // "x.3a : non 45 degree angle m5"
 // "x.3a : non 45 degree angle ncm"
 // "x.3a : non 45 degree angle npc"
 // "x.3a : non 45 degree angle nsdm"
 // "x.3a : non 45 degree angle nsm"
 // "x.3a : non 45 degree angle nwell"
 // "x.3a : non 45 degree angle pad"
 // "x.3a : non 45 degree angle psdm"
 // "x.3a : non 45 degree angle pwbm"
 // "x.3a : non 45 degree angle pwde"
 // "x.3a : non 45 degree angle pwell_rs"
 // "x.3a : non 45 degree angle rpm"
 // "x.3a : non 45 degree angle tunm"
 // "x.3a : non 45 degree angle uhvi"
 // "x.3a : non 45 degree angle vhvi"
 // "x.3a : non 45 degree angle vpp"

//set_die_area 0 0 106060 106060

density_rule "min_fail" {
caption "Min Fail"
density_layer MET1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 1000 BY 1000
density_step 1001
density_exclude   MET2
density_maximum 0.0
density_minimum 0.10
density_surround 10
density_mode TEST
density_report TEST1
density_min_fail

}


density_rule "max_fail" {
caption "Max Fail"
density_layer MET1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 1000 BY 1000
density_step 1001
density_exclude   MET2
density_maximum 0.30
density_minimum 0.50
density_surround 10
density_mode TEST
density_report TEST1
density_max_fail

}
```

```
density_rule "out_of_range" {
caption "Out of Range"
density_layer MET1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 1000 BY 1000
density_step 1001
density_exclude   MET2
density_maximum 0.30
density_minimum 0.30
density_surround 10
density_mode TEST
density_report TEST1
density_out_of_range

}


density_rule "xdir_fail" {
caption "Xdir fail"
density_layer MET1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 1000 BY 1000
density_step 1001
density_exclude   MET2
density_maximum 0.30
density_minimum 0.30
density_surround 10
density_mode TEST
density_report TEST1
density_xdir_fail

}


density_rule "ydir_fail" {
caption "Ydir Fail"
density_layer MET1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 1000 BY 1000
density_step 1001
density_exclude   MET2
density_maximum 0.30
density_minimum 0.10
density_surround 10
density_mode TEST
density_report TEST1
density_ydir_fail

}

// below are 3nm rules




//# ===== METAL 1: width/space/area/EOL/notch/jog =====
//RULE_001: M1 WIDTH < 18nm              -> ERR "M1_MIN_WIDTH"
//RULE_002: M1 SPACE < 20nm DIFF_NET     -> ERR "M1_MIN_SPACE_DIFF"
//RULE_003: M1 SPACE < 18nm SAME_NET     -> ERR "M1_MIN_SPACE_SAME"
```

```
//RULE_004: M1 AREA  < 32nm^2            -> ERR "M1_MIN_AREA"
//RULE_005: M1 EOL_SPACE < 24nm LEN<30nm -> ERR "M1_EOL_SPACE"
//RULE_006: M1 NOTCH < 16nm DEPTH>16nm   -> ERR "M1_NOTCH"
//RULE_007: M1 JOG_LEN < 24nm            -> ERR "M1_MIN_JOG_LEN"
//RULE_008: M1 CORNER_ANGLE < 70deg      -> ERR "M1_ACUTE_ANGLE"
//
//# ===== METAL 2: pitch/color/EUV/forbidden =====
//RULE_009: M2 WIDTH < 18nm              -> ERR "M2_MIN_WIDTH"
//RULE_010: M2 PITCH < 36nm              -> ERR "M2_MIN_PITCH"
//RULE_011: M2 SPACE_COLOR SAME < 18nm   -> ERR "M2_SAMECOLOR_SPACE"
//RULE_012: M2 SPACE_COLOR DIFF < 16nm   -> ERR "M2_DIFCOLOR_SPACE"
//RULE_013: M2 FORBIDDEN_PITCH {44, 52}  -> ERR "M2_FORBIDDEN_PITCH"
//RULE_014: M2 ODD_CYCLE DETECT          -> ERR "M2_ODD_CYCLE"
//RULE_015: M2 LINE_END_TO_EDGE < 22nm   -> ERR "M2_TIP_TO_EDGE"
//RULE_016: M2 BLOCK_MASK_SPACE < 40nm   -> ERR "M2_BLOCK_SPACE"
//
//# ===== METAL 3: multi-patterning & EOL variants =====
//RULE_017: M3 WIDTH < 20nm              -> ERR "M3_MIN_WIDTH"
//RULE_018: M3 SPACE < 22nm DIFF_NET     -> ERR "M3_MIN_SPACE"
//RULE_019: M3 COLORING REQUIRED         -> ERR "M3_UNCOLORED"
//RULE_020: M3 SAME_COLOR_CHAIN LEN>1um  -> ERR "M3_SAMECOLOR_CHAIN_LEN"
//RULE_021: M3 EOL_EXT < 14nm            -> ERR "M3_MIN_EOL_EXT"
//RULE_022: M3 TIP2TIP < 20nm            -> ERR "M3_TIP2TIP"
//
//# ===== CUT/VIA layers =====
//RULE_023: VIA1 CUT_WIDTH < 12nm        -> ERR "V1_MIN_CUT_WIDTH"
//RULE_024: VIA1 CUT_SPACE  < 36nm       -> ERR "V1_MIN_CUT_SPACE"
//RULE_025: VIA1 ENCLOSED_BY M1 < 10nm   -> ERR "V1_ENC_M1"
//RULE_026: VIA1 ENCLOSED_BY M2 < 10nm   -> ERR "V1_ENC_M2"
//RULE_027: VIA1 TO M1 EDGE < 6nm        -> ERR "V1_TO_M1_EDGE"
//RULE_028: VIA1 ARRAY PITCH_XY < (36,36)-> ERR "V1_ARRAY_PITCH"
//RULE_029: VIA1 STACKED W/ VIA2 RESTRICT-> ERR "V1_V2_STACK_RULE"
//RULE_030: VIA2 CUT_SPACE < 40nm        -> ERR "V2_MIN_CUT_SPACE"
//
//# ===== LI / LOCAL INTERCONNECT / CONTACT =====
//RULE_031: LI WIDTH < 14nm              -> ERR "LI_MIN_WIDTH"
//RULE_032: LI SPACE < 16nm              -> ERR "LI_MIN_SPACE"
//RULE_033: CONTACT_OD ENC < 8nm         -> ERR "CONT_OD_ENC"
//RULE_034: CONTACT_PO ENC < 8nm         -> ERR "CONT_PO_ENC"
//
//# ===== POLY / GATE (FEOL) =====
//RULE_035: POLY WIDTH < 14nm            -> ERR "PO_MIN_WIDTH"
//RULE_036: POLY SPACE < 18nm            -> ERR "PO_MIN_SPACE"
//RULE_037: GATE_LENGTH < 16nm           -> ERR "GATE_MIN_L"
//RULE_038: POLY_TO_OD < 8nm             -> ERR "PO_TO_OD_SPACE"
//RULE_039: POLY_JOG_LEN < 20nm          -> ERR "PO_MIN_JOG_LEN"
//
//# ===== ACTIVE / OD / DIFF =====
//RULE_040: OD AREA < 40nm^2             -> ERR "OD_MIN_AREA"
//RULE_041: OD NOTCH < 16nm DEPTH>16nm   -> ERR "OD_NOTCH"
//RULE_042: OD TO OD SPACE < 20nm        -> ERR "OD_MIN_SPACE"
//
//# ===== WELL / IMPLANT =====
//RULE_043: NWELL TO PWELL < 60nm        -> ERR "WELL_ABUT_SPACE"
//RULE_044: IMPLANT OVERLAP OD < 6nm     -> ERR "IMP_OD_OVERLAP"
//RULE_045: WELL_TAP_DENSITY WIN 1um <1/5-> ERR "WELL_TAP_DENSITY"
//
//# ===== DENSITY / CMP =====
//RULE_046: M1 DENSITY WIN 500x500nm 20{80%  -> ERR "M1_DENSITY_RANGE"
//RULE_047: M1 DENSITY_GRAD ADJ_WIN > 15%    -> ERR "M1_DENSITY_GRAD"
//RULE_048: {M1+M2} COMBO_DENS WIN 1x1um 30{70% -> ERR "MX_COMBO_DENS"
//RULE_049: SLOT_REQUIRED WIDTH>200nm SLOT_W=40nm S=80nm -> ERR "M1_SLOT_REQ"
```

```
//
//# ===== DFM-style recommended (flag as WARN unless strict) =====
//RULE_050: VIA_REDUNDANCY REQ ON CRIT_NET -> WARN "VIA_REDUNDANCY_REQ"
```

2.2 NG45.lrf example

```
lvr_layer_map 1 -datatype 0 30000
lvr_layer_def active 30000
lvr_layer_map 2 -datatype 0 30005
lvr_layer_def pwell 30005
lvr_layer_map 3 -datatype 0 30010
lvr_layer_def nwell 30010
lvr_layer_map 4 -datatype 0 30015
lvr_layer_def nplus 30015
lvr_layer_map 5 -datatype 0 30020
lvr_layer_def pplus 30020
lvr_layer_map 6 -datatype 0 30025
lvr_layer_def vtg 30025
lvr_layer_map 7 -datatype 0 30030
lvr_layer_def vth 30030
lvr_layer_map 8 -datatype 0 30035
lvr_layer_def thkox 30035
lvr_layer_map 9 -datatype 0 30040
lvr_layer_def poly 30040
lvr_layer_map 10 -datatype 0 30045
lvr_layer_def cont 30045
lvr_layer_map 11 -datatype 0 30050
lvr_layer_def metal1 30050
lvr_layer_map 11 -texttype 0 30051
lvr_layer_def metal1_txt 30051
lvr_layer_map 12 -datatype 0 30055
lvr_layer_def via1 30055
lvr_layer_map 13 -datatype 0 30060
lvr_layer_def metal2 30060
lvr_layer_map 13 -texttype 0 30061
lvr_layer_def metal2_txt 30061
lvr_layer_map 14 -datatype 0 30065
lvr_layer_def via2 30065
lvr_layer_map 15 -datatype 0 30070
lvr_layer_def metal3 30070
lvr_layer_map 16 -datatype 0 30075
lvr_layer_def via3 30075
lvr_layer_map 17 -datatype 0 30080
lvr_layer_def metal4 30080
lvr_layer_map 18 -datatype 0 30085
lvr_layer_def via4 30085
lvr_layer_map 19 -datatype 0 30090
lvr_layer_def metal5 30090
lvr_layer_map 20 -datatype 0 30095
lvr_layer_def via5 30095
lvr_layer_map 21 -datatype 0 30100
lvr_layer_def metal6 30100
lvr_layer_map 22 -datatype 0 30105
lvr_layer_def via6 30105
lvr_layer_map 23 -datatype 0 30110
lvr_layer_def metal7 30110
lvr_layer_map 24 -datatype 0 30115
lvr_layer_def via7 30115
lvr_layer_map 25 -datatype 0 30120
lvr_layer_def metal8 30120
lvr_layer_map 26 -datatype 0 30125
lvr_layer_def via8 30125
lvr_layer_map 27 -datatype 0 30130
lvr_layer_def metal9 30130
lvr_layer_map 28 -datatype 0 30135
lvr_layer_def via9 30135
```

```
lvr_layer_map 29 -datatype 0 30140
lvr_layer_def metal10 30140
lvr_layer_map 63 -texttype 63 30141
lvr_layer_def metal11 30141
lvr_layer_map 63 -datatype 0 30142
lvr_layer_def metal12 30142
lvr_layer_map 235 -datatype 0 30143
lvr_layer_def metal13 30143

//size ( extent ) -by 1.0 -layerOut bulk
//not bulk nwell -layerOut PWELL

and poly active -layerOut gate
//add below in the code, not here
and active nplus -layerOut ndiff
and active pplus -layerOut pdiff
and cont active -layerOut diode

or poly poly -layerOut MYPOLY
or ndiff pdiff -layerOut MYDIFF

connect metal1 metal1_txt
connect metal1 metal1
connect metal2 metal2_txt
connect metal2 metal2
connect via2 metal3
connect metal2 via2
connect via1 metal2
connect metal1 via1
connect cont metal1
connect MYDIFF cont
connect MYPOLY cont

lvs_timeout 10
lvs_max_error 100

drc_rule "well.1" {
  caption "well.1 : nwell/pwell must not overlap"
  and well well
}
drc_rule "well.3" {
  caption "well.3 : minimum  spacing of nwell at same potential : 135nm"
   spacing -same_layer well well -lt 0.135
}
drc_rule "well.3" {
  caption "well.3 : minimum  spacing of pwell at same potential : 135nm"
   spacing -same_layer well well -lt 0.135
}
drc_rule "well.4" {
  caption "well.4 : minimum width of nwell/pwell : 200nm"
  edge_width well -lt 0.2
}
drc_rule "vt.1" {
  caption "vt.1 : vtg adjust layers must coincide with well"
  not well vt
}
drc_rule "vt.1" {
  caption "vt.1 : vth adjust layers must coincide with well"
  not well vt
}
drc_rule "poly.1" {
  caption "poly.1 : minimum width of poly : 50nm"
```

```
  edge_width poly -lt 0.05
}
drc_rule "poly.2.a" {
  caption "poly.2 : minimum  spacing of poly and active: 140nm"
   spacing -same_layer active active -lt 0.04
}
drc_rule "poly.2.b" {
  caption "poly.2 : minimum  spacing of poly and active: 140nm"
   spacing -same_layer poly poly -lt 0.04
}
drc_rule "poly.3" {
  caption "poly.3 : minimum poly extension beyond active : 55nm"
  extension active poly -lt 0.055
}
drc_rule "poly.4" {
  caption "poly.4 : minimum enclosure of active around gate : 70nm"
  and active gate -layerOut gate_active
  enclosure -opposite_side gate_active active -lt 0.07
}
drc_rule "poly.5" {
  caption "poly.5 : minimum  spacing of field poly to active: 50nm"
   spacing active poly -lt 0.05
}
drc_rule "poly.6" {
  caption "poly.6 : minimum  spacing of field poly: 75nm"
   spacing -same_layer poly poly -lt 0.075
}
drc_rule "active.1" {
  caption "active.1 : minimum width of active : 90nm"
  edge_width active -lt 0.09
}
drc_rule "active.2" {
  caption "active.2 : minimum  spacing of active : 80nm"
   spacing -same_layer active active -lt 0.08
}
drc_rule "active.3" {
  caption "active.3 : minimum enclosure/ spacing of nwell/pwell to active: 55nm"
  enclosure -all_side active well -lt 0.055
}
drc_rule "active.4" {
  caption "active.4 : active must be inside nwell or pwell"
  not active well
}
drc_rule "implant.1" {
  caption "implant.1 : minimum  spacing of nimplant/ pimplant to channel : 70nm"
   spacing implant implant -lt 0.07
}
drc_rule "implant.2" {
  caption "implant.1 : minimum  spacing of nimplant/ pimplant to contact : 25nm"
   spacing contact implant -lt 0.025
}
drc_rule "implant.3" {
  caption "implant.3 : minimum width of nimplant/ pimplant  : 45nm"
  edge_width implant -lt 0.045
}
drc_rule "implant.4" {
  caption "implant.4 : minimum  spacing of nimplant/ pimplant  : 45nm"
   spacing implant implant -lt 0.045
}
drc_rule "implant.5" {
  caption "implant.5 : nimplant and pimplant must not overlap"
  and implant implant
```

```
}
drc_rule "contact.1" {
  caption "contact.1 : minimum/maximum width of contact : 65nm"
  edge_width contact -gt 0.065
}
drc_rule "contact.2" {
  caption "contact.2 : minimum  spacing of contact : 75nm"
   spacing -same_layer contact contact -lt 0.075
}
drc_rule "contact.3" {
  caption "contact.3 : contact must be inside active or poly or metal1"
  not contact active
}
drc_rule "contact.4" {
  caption "contact.4 : minimum enclosure of active around contact : 5nm"
  enclosure -all_side contact active -lt 0.005
}
drc_rule "contact.5" {
  caption "contact.5 : minimum enclosure of poly around contact : 5nm"
  enclosure -all_side contact poly -lt 0.005
}
drc_rule "contact.6" {
  caption "contact.6 : minimum  spacing of contact and poly : 35nm"
   spacing contact poly -lt 0.035
}
drc_rule "metal1.1" {
  caption "metal1.1 : minimum width of metal1 : 65nm"
  edge_width metal1 -lt 0.065
}
drc_rule "metal1.2" {
  caption "metal1.2 : minimum  spacing of metal1 : 65nm"
   spacing -same_layer metal1 metal1 -lt 0.065
}
drc_rule "metal1.3" {
  caption "metal1.3 : minimum enclosure around contact on two opposite sides : 35nm"
  enclosure -opposite_side contact metal1 -lt 0.035
}
drc_rule "metal1.4" {
  caption "metal1.4 : minimum enclosure around via1 on two opposite sides : 35nm"
  enclosure -opposite_side via1 metal1 -lt 0.035
}
drc_rule "metal1.5" {
  caption "metal1.5 : minimum  spacing of metal1 wider than 90 nm and longer than 300 nm : 90nm"
 spacing  -wider 0.09  -longer 0.3 -same_layer metal1 metal1 -lt 0.09
}
drc_rule "metal1.6" {
  caption "metal1.6 : minimum  spacing of metal1 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal1 metal1 -lt 0.27
}
drc_rule "metal1.7" {
  caption "metal1.7 : minimum  spacing of metal1 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.5  -longer 1.8 -same_layer metal1 metal1 -lt 0.5
}
drc_rule "metal1.8" {
  caption "metal1.8 : minimum  spacing of metal1 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal1 metal1 -lt 0.9
}
drc_rule "metal1.9" {
  caption "metal1.9 : minimum  spacing of metal1 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal1 metal1 -lt 1.5
}
drc_rule "via1.1" {
```

```
  caption "via1.1 : minimum/maximum width of via1 : 65nm"
  edge_width via1 -lt 0.065
}
drc_rule "via1.2" {
  caption "via1.2 : minimum  spacing of via1 : 75nm"
   spacing -same_layer via1 via1 -lt 0.075
}
drc_rule "via1.3" {
  caption "via1.3 : via1 must be inside metal1"
  not via1 metal1
}
drc_rule "via1.4" {
  caption "via1.4 : via1 must be inside metal2"
  not via1 metal2
}
drc_rule "metal2.1" {
  caption "metal2.1 : minimum width of  intermediate metal2 : 70nm"
  edge_width metal2 -lt 0.07
}
drc_rule "metal2.2" {
  caption "metal2.2 : minimum  spacing of  intermediate metal2 : 70nm"
   spacing -same_layer metal2 metal2 -lt 0.07
}
drc_rule "metal2.3" {
  caption "metal2.3 : minimum enclosure around via1 on two opposite sides : 35nm"
  enclosure -opposite_side via1 metal2 -lt 0.035
}
drc_rule "metal2.4" {
  caption "metal2.4 : minimum enclosure around via2 on two opposite sides : 35nm"
  enclosure -opposite_side via2 metal2 -lt 0.035
}
drc_rule "metal2.5" {
  caption "metal2.5 : minimum  spacing of  intermediate metal2 wider than 90 nm and longer than 300 nm : 90nm"
 spacing  -wider 0.9  -longer 0.3 -same_layer metal2 metal2 -lt 0.09
}
drc_rule "metal2.6" {
  caption "metal2.6 : minimum  spacing of  intermediate metal2 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal2 metal2 -lt 0.27
}
drc_rule "metal2.7" {
  caption "metal2.7 : minimum  spacing of  intermediate metal2 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal2 metal2 -lt 0.500
}
drc_rule "metal2.8" {
  caption "metal2.8 : minimum  spacing of  intermediate metal2 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal2 metal2 -lt 0.9
}
drc_rule "metal2.9" {
  caption "metal2.9 : minimum  spacing of  intermediate metal2 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal2 metal2 -lt 1.5
}
drc_rule "via2.1" {
  caption "via2.1 : minimum/maximum width of via2 : 70nm"
  edge_width via2 -gt 0.07
}
drc_rule "via2.2" {
  caption "via2.2 : minimum  spacing of via2 : 85nm"
   spacing -same_layer via2 via2 -lt 0.085
}
drc_rule "via2.3" {
  caption "via2.3 : via2 must be inside metal2"
  not via2 metal2
```

```
}
drc_rule "via2.4" {
  caption "via2.4 : via2 must be inside metal3"
  not via2 metal3
}
drc_rule "metal3.1" {
  caption "metal3.1 : minimum width of  intermediate metal3 : 70nm"
  edge_width metal3 -lt 0.07
}
drc_rule "metal3.2" {
  caption "metal3.2 : minimum  spacing of  intermediate metal3 : 70nm"
   spacing -same_layer metal3 metal3 -lt 0.07
}
drc_rule "metal3.3" {
  caption "metal3.3 : minimum enclosure around via2 on two opposite sides : 35nm"
  enclosure -opposite_side via2 metal3 -lt 0.035
}
drc_rule "metal3.4" {
  caption "metal3.4 : minimum enclosure around via3 on two opposite sides : 35nm"
  enclosure -opposite_side via3 metal3 -lt 0.035
}
drc_rule "metal3.5" {
  caption "metal3.5 : minimum  spacing of  intermediate metal3 wider than 90 nm and longer than 300 nm : 90nm"
 spacing  -wider 0.9  -longer 0.3 -same_layer metal3 metal3 -lt 0.9
}
drc_rule "metal3.6" {
  caption "metal3.6 : minimum  spacing of  intermediate metal3 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal3 metal3 -lt 0.27
}
drc_rule "metal3.7" {
  caption "metal3.7 : minimum  spacing of  intermediate metal3 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal3 metal3 -lt 0.50
}
drc_rule "metal3.8" {
  caption "metal3.8 : minimum  spacing of  intermediate metal3 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal3 metal3 -lt 0.9
}
drc_rule "metal3.9" {
  caption "metal3.9 : minimum  spacing of  intermediate metal3 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal3 metal3 -lt 0.1500
}
drc_rule "via3.1" {
  caption "via3.1 : minimum/maximum width of via3 : 70nm"
  edge_width via3 -gt 0.07
}
drc_rule "via3.2" {
  caption "via3.2 : minimum  spacing of via3 : 85nm"
   spacing -same_layer via3 via3 -lt 0.085
}
drc_rule "via3.3" {
  caption "via3.3 : via3 must be inside metal3"
  not via3 metal3
}
drc_rule "via3.4" {
  caption "via3.4 : via3 must be inside metal4"
  not via3 metal4
}
drc_rule "metal4.1" {
  caption "metal4.1 : minimum width of  semi-global metal4 : 140nm"
  edge_width metal4 -lt 0.14
}
drc_rule "metal4.2" {
```

```
  caption "metal4.2 : minimum  spacing of  semi-global metal4 : 140nm"
   spacing -same_layer metal4 metal4 -lt 0.14
}
drc_rule "metal4.6" {
  caption "metal4.6 : minimum  spacing of semi-global metal4 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal4 metal4 -lt 0.27
}
drc_rule "metal4.7" {
  caption "metal4.7 : minimum  spacing of semi-global metal4 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal4 metal4 -lt 0.500
}
drc_rule "metal4.8" {
  caption "metal4.8 : minimum  spacing of semi-global meta4l wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal4 metal4 -lt 0.9
}
drc_rule "via4.1" {
  caption "via4.1 : minimum width of via4 : 140nm"
  edge_width via4 -lt 0.14
}
drc_rule "via4.2" {
  caption "via4.2 : minimum  spacing of via4 : 160nm"
   spacing via4 via4 -lt 0.16
}
drc_rule "via4.3" {
  caption "via4.3 : via4 must be inside metal4"
  not via4 metal4
}
drc_rule "via4.4" {
  caption "via4.4 : via4 must be inside metal5"
  not via4 metal5
}
drc_rule "metal5.1" {
  caption "metal5.1 : minimum width of semi-global metal5 : 140nm"
  edge_width metal5 -lt 0.14
}
drc_rule "metal5.2" {
  caption "metal5.2 : minimum  spacing of semi-global metal5 : 140nm"
   spacing -same_layer metal5 metal5 -lt 0.14
}
drc_rule "metal5.6" {
  caption "metal5.6 : minimum  spacing of semi-global metal5 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal5 metal5 -lt 0.27
}
drc_rule "metal5.7" {
  caption "metal5.7 : minimum  spacing of semi-global metal5 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal5 metal5 -lt 0.50
}
drc_rule "metal5.8" {
  caption "metal5.8 : minimum  spacing of semi-global meta5l wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal5 metal5 -lt 0.9
}
drc_rule "via5.1" {
  caption "via5.1 : minimum/maximum width of via5 : 140nm"
  edge_width via5 -gt 0.14
}
drc_rule "via5.2" {
  caption "via5.2 : minimum  spacing of via5 : 160nm"
   spacing -same_layer via5 via5 -lt 0.16
}
drc_rule "via5.3" {
  caption "via5.3 : via5 must be inside metal5"
  not via5 metal5
```

```
}
drc_rule "via5.4" {
  caption "via5.4 : via5 must be inside metal6"
  not via5 metal6
}
drc_rule "metal6.1" {
  caption "metal6.1 : minimum width of semi-global metal6 : 140nm"
  edge_width metal6 -lt 0.14
}
drc_rule "metal6.2" {
  caption "metal6.2 : minimum  spacing of semi-global metal6 : 140nm"
   spacing -same_layer metal6 metal6 -lt 0.14
}
drc_rule "metal6.6" {
  caption "metal6.6 : minimum  spacing of semi-global metal6 wider than 270 nm and longer than 900 nm : 270nm"
 spacing  -wider 0.27  -longer 0.9 -same_layer metal6 metal6 -lt 0.27
}
drc_rule "metal6.7" {
  caption "metal6.7 : minimum  spacing of semi-global metal6 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal6 metal6 -lt 0.50
}
drc_rule "metal6.8" {
  caption "metal6.8 : minimum  spacing of semi-global metal6 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.90  -longer 2.7 -same_layer metal6 metal6 -lt 0.9
}
drc_rule "via6.1" {
  caption "via6.1 : minimum/maximum width of via6 : 140nm"
  edge_width via6 -gt 0.14
}
drc_rule "via6.2" {
  caption "via6.2 : minimum  spacing of via6 : 160nm"
   spacing -same_layer via6 via6 -lt 0.16
}
drc_rule "via6.3" {
  caption "via6.3 : via6 must be inside metal6"
  not via6 metal6
}
drc_rule "via6.4" {
  caption "via6.4 : via6 must be inside metal7"
  not via6 metal7
}
drc_rule "metal7.1" {
  caption "metal7.1 : minimum width of thin global metal7 : 400nm"
  edge_width metal7 -lt 0.4
}
drc_rule "metal7.2" {
  caption "metal7.2 : minimum  spacing of thin global metal7 : 400nm"
   spacing -same_layer metal7 metal7 -lt 0.4
}
drc_rule "metal7.7" {
  caption "metal7.7 : minimum  spacing of thin global metal7 wider than 500 nm and longer than 1.8 um : 500nm"
   spacing  -wider 0.50  -longer 1.8 -same_layer metal7 metal7 -lt 0.50
}
drc_rule "metal7.8" {
  caption "metal7.8 : minimum  spacing of thin global metal7 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal7 metal7 -lt 0.9
}
drc_rule "metal7.9" {
  caption "metal7.9 : minimum  spacing of thin global meta7l wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal7 metal7 -lt 1.50
}
drc_rule "via7.1" {
```

```
  caption "via6.1 : minimum/maximum width of via7 : 400nm"
  edge_width via7 -gt 0.4
}
drc_rule "via7.2" {
  caption "via6.7 : minimum  spacing of via7 : 440nm"
   spacing -same_layer via7 via7 -lt 0.44
}
drc_rule "via7.3" {
  caption "via7.3 : via7 must be inside metal7"
  not via7 metal7
}
drc_rule "via7.4" {
  caption "via7.4 : via7 must be inside metal8"
  not via7 metal8
}
drc_rule "metal8.1" {
  caption "metal8.1 : minimum width of thin global metal8 : 400nm"
  edge_width metal8 -lt 0.4
}
drc_rule "metal8.2" {
  caption "metal8.2 : minimum  spacing of thin global metal8 : 400nm"
   spacing -same_layer metal8 metal8 -lt 0.4
}
drc_rule "metal8.7" {
  caption "metal8.7 : minimum  spacing of thin global metal8 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.5  -longer 1.8 -same_layer metal8 metal8 -lt 0.5
}
drc_rule "metal8.8" {
  caption "metal8.8 : minimum  spacing of thin global metal8 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal8 metal8 -lt 0.9
}
drc_rule "metal8.9" {
  caption "metal8.9 : minimum  spacing of thin global metal8 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal8 metal8 -lt 1.5
}
drc_rule "via8.1" {
  caption "via8.1 : minimum/maximum width of via8 : 400nm"
  edge_width via8 -gt 0.4
}
drc_rule "via8.2" {
  caption "via8.2 : minimum  spacing of via8 : 440nm"
   spacing -same_layer via8 via8 -lt 0.44
}
drc_rule "via8.3" {
  caption "via8.3 : via8 must be inside metal8"
  not metal8 via8
}
drc_rule "via8.4" {
  caption "via8.4 : via8 must be inside metal9"
  not metal9 via8
}
drc_rule "metal9.1" {
  caption "metal9.1 : minimum width of global metal9 : 800nm"
  edge_width metal9 -lt 0.8
}
drc_rule "metal9.2" {
  caption "metal9.2 : minimum  spacing of global metal9 : 800nm"
   spacing -same_layer metal9 metal9 -lt 0.8
}
drc_rule "metal9.7" {
  caption "metal9.7 : minimum  spacing of global metal9 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.5  -longer 1.8 -same_layer metal9 metal9 -lt 0.5
```

```
}
drc_rule "metal9.8" {
  caption "metal9.8 : minimum  spacing of global metal9 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal9 metal9 -lt 0.9
}
drc_rule "metal9.9" {
  caption "metal9.9 : minimum  spacing of global metal9 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal9 metal9 -lt 1.5
}
drc_rule "via9.1" {
  caption "via9.1 : minimum/maximum width of via9 : 800nm"
  edge_width via9 -gt 0.8
}
drc_rule "via9.2" {
  caption "via9.2 : minimum  spacing of via9 : 880nm"
   spacing -same_layer via9 via9 -lt 0.88
}
drc_rule "via9.3" {
  caption "via9.3 : via9 must be inside metal9"
  not metal9 via9
}
drc_rule "via9.4" {
  caption "via9.4 : via9 must be inside metal10"
  not metal10 metal1
}
drc_rule "metal10.1" {
  caption "metal10.1 : minimum width of global metal10 : 800nm"
  edge_width metal10 -lt 0.8
}
drc_rule "metal10.2" {
  caption "metal10.2 : minimum  spacing of global metal10 : 800nm"
   spacing -same_layer metal10 metal10 -lt 0.8
}
drc_rule "metal10.7" {
  caption "metal10.7 : minimum  spacing of global metal10 wider than 500 nm and longer than 1.8 um : 500nm"
 spacing  -wider 0.50  -longer 1.8 -same_layer metal10 metal10 -lt 0.50
}
drc_rule "metal10.8" {
  caption "metal10.8 : minimum  spacing of global metal10 wider than 900 nm and longer than 2.7 um : 900nm"
 spacing  -wider 0.9  -longer 2.7 -same_layer metal10 metal10 -lt 0.9
}
drc_rule "metal10.9" {
  caption "metal10.9 : minimum  spacing of global metal10 wider than 1500 nm and longer than 4.0 um : 1500nm"
 spacing  -wider 1.5  -longer 4.0 -same_layer metal10 metal10 -lt 1.5
}
drc_rule "metal1_antenna" {
  caption "metal1_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal2_antenna" {
  caption "metal2_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal3_antenna" {
  caption "metal3_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal4_antenna" {
  caption "metal4_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal5_antenna" {
```

```
  caption "metal5_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal6_antenna" {
  caption "metal6_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal7_antenna" {
  caption "metal7_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal8_antenna" {
  caption "metal8_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal9_antenna" {
  caption "metal9_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}
drc_rule "metal10_antenna" {
  caption "metal10_antenna : ratio of maximum allowed (field poly area or metal layer area) to transistor gate area : 300:1"
  // todo: drc_rule for this caption
}

density_rule "min_fail" {
caption "Min Fail"
density_layer metal1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 10000 BY 10000
density_step 10001
density_exclude   metal2
density_maximum 0.0
density_minimum 0.10
density_surround 10
density_mode TEST
density_report TEST1
density_min_fail

}


density_rule "max_fail" {
caption "Max Fail"
density_layer metal1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 10000 BY 10000
density_step 10001
density_exclude   metal2
density_maximum 0.30
density_minimum 0.50
density_surround 10
density_mode TEST
density_report TEST1
density_max_fail

}


density_rule "out_of_range" {
caption "Out of Range"
```

```
density_layer metal1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 10000 BY 10000
density_step 10001
density_exclude   metal2
density_maximum 0.30
density_minimum 0.30
density_surround 10
density_mode TEST
density_report TEST1
density_out_of_range

}


density_rule "xdir_fail" {
caption "Xdir fail"
density_layer metal1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 10000 BY 10000
density_step 10001
density_exclude   metal2
density_maximum 0.30
density_minimum 0.30
density_surround 10
density_mode TEST
density_report TEST1
density_xdir_fail

}


density_rule "ydir_fail" {
caption "Ydir Fail"
density_layer metal1
//density_window SIZE 10606 BY 10606
//density_window SIZE 106060 BY 106060
density_window SIZE 10000 BY 10000
density_step 10001
density_exclude   metal2
density_maximum 0.30
density_minimum 0.10
density_surround 10
density_mode TEST
density_report TEST1
density_ydir_fail

}
```