Capability Statement (Revised)

Ramtera Inc. — Large-Scale Distributed Physical Verification

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Company Overview

Ramtera Inc. is a Delaware-registered U.S. semiconductor software company founded in 2024 with a mission to advance the frontiers of physical verification and design sign-off for the global semiconductor industry. The company focuses on architectural solutions to the scalability limitations faced by traditional electronic design automation (EDA) tools as layout complexity continues to grow.

Ramtera's flagship product, **LVR (Layout Verification Reporter)**, is a distributed, cloud-native physical verification platform supporting Design Rule Checking (DRC), Layout Versus Schematic (LVS), Electrical Rule Checking (ERC), Density, XOR, and Design-for-Manufacturability (DFM) analysis. LVR is architected from the ground up for large-scale geometric workloads, emphasizing predictable runtime behavior, memory efficiency, and reproducibility on commodity cluster infrastructure.

At its core, Ramtera's philosophy is that future physical-verification systems must rely on fundamental architectural redesign rather than incremental optimization. The goal is to make verification at extreme scale routine and economically viable.

Vision and Mission

Ramtera's mission is to democratize high-performance physical-verification capability for design teams of every scale—from emerging fabless startups to Tier-1 semiconductor foundries.

The company's guiding principle is *verification at any scale*: no design, however large or hierarchical, should be constrained by tool capacity, license fragmentation, or infrastructure limitations. In the context of chiplets, 3D IC, and heterogeneous integration, Ramtera aims to redefine what constitutes practical sign-off capacity.

Core Product — Layout Verification Reporter (LVR)

LVR unifies multiple sign-off verification functions into a single scalable execution engine with a common internal geometry and connectivity representation. The platform supports industry-

standard formats including GDS II, OASIS, SPICE, and Verilog, and provides both GUI-based debugging and TCL-based scripting interfaces for automation.

Architecture Overview

- **Multi-Threaded Core:** Implemented in modern C++ with task-based scheduling for near-linear scaling across CPU cores.
- **Distributed Execution:** Spatial partitioning based on R-tree indexing enables data-parallel verification across multiple nodes.
- **Memory Efficiency:** Boundary-only polygon representation and custom geometric containers significantly reduce memory footprint.
- **Cross-Platform Support:** Production binaries for Ubuntu, Red Hat Enterprise Linux, and macOS.

Key Capabilities

- DRC: Width, spacing, enclosure, and density checks
- LVS: Flat and hierarchical comparison with device recognition
- ERC: Shorts, opens, and power/ground connectivity validation
- Density and DFM: Local window analysis and manufacturability checks
- XOR: Fast regression and ECO validation
- ECO Editing: Polygon modification and GDS export

Measured Performance and Scalability

Ramtera has recently completed a series of controlled distributed-execution experiments to characterize LVR's runtime scaling behavior as a function of layout size.

Experimental Configuration

- Cluster size: 128 nodes
- Total CPU cores: 1024
- Execution mode: Distributed, flattened layouts
- Rule categories: Density, XOR, Width, Enclosure, Spacing, and full rule deck

All experiments were executed with identical hardware and software configurations.

Table 1: LVR Results on Distributed Computing for 1 Billion Polygon Design

Module	Design Size	Num Cores	Num Nodes	Runtime (seconds)
Min Density	1 Billion Polygons	1024	128	36 seconds
Max Density	1 Billion Polygons	1024	128	36 seconds
Min-Max Density	1 Billion Polygons	1024	128	36 seconds
XOR	1 Billion Polygons	1024	128	74 seconds
Width	1 Billion Polygons	1024	128	34 seconds
Enclosure	1 Billion Polygons	1024	128	35 seconds
Spacing	1 Billion Polygons	1024	128	34 seconds
346 rules	1 Billion Polygons	1024	128	38 seconds

Table 2: LVR Results on Distributed Computing for 10 Billion Polygon Design

Module	Design Size	Num Cores	Num Nodes	Runtime (minutes)
Min Density	10 Billion Polygons	1024	128	7 min 26 seconds
Max Density	10 Billion Polygons	1024	128	7 min 29 seconds
Min-Max Density	10 Billion Polygons	1024	128	7 min 25 seconds
XOR	10 Billion Polygons	1024	128	OOM
Width	10 Billion Polygons	1024	128	7 min 34 seconds
Enclosure	10 Billion Polygons	1024	128	7 min 19 seconds
Spacing	10 Billion Polygons	1024	128	7 min 16 seconds
346 rules	10 Billion Polygons	1024	128	7 min 36 seconds

Runtime Results

Observations

Based strictly on measured data:

- A 10× increase in polygon count results in an approximately 10× increase in runtime.
- Scaling behavior is consistent across different rule categories.
- No super-linear runtime growth was observed up to 100 billion polygons under fixed compute.

These results indicate approximately linear runtime scaling with respect to polygon count for the evaluated configuration.

Technology Node Coverage

LVR has been validated on multiple technology nodes spanning from 180 nm to 15 nm, including Sky130HD, XH018, NG45, NG15, and SAED32. Additional nodes are under active qualification, covering both open-source and NDA-based process design kits.

Intellectual Property

- 4 USPTO patents (provisional / utility pending)

- 4 Indian patents (granted)
- 12 registered technical documents and manuals
- Registered trademark: *LVR — Layout Verification Reporter*

All intellectual property is owned by Ramtera Inc. (USA), with full assignment from its Indian subsidiary.

Summary

Ramtera Inc. has progressed from early-stage scalability demonstrations to measured, multi-decade runtime scaling on distributed infrastructure. The results presented in this capability statement establish LVR as a technically credible platform for large-scale physical verification workloads and motivate further evaluation in cloud- and infrastructure-centric environments.