RAMTERA

PRODUCT DOCUMENTATION · PHYSICAL VERIFICATION (LVR)

RAMTERA-LVR-DS

LVR Product Datasheet

DRC · LVS · ERC · XOR · PEX — one engine, native rule decks, pre-signoff economics

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LVR — Layout Verification Reporter

LVR is Ramtera's physical verification platform: design rule checking (DRC), layout-versus-schematic (LVS), electrical rule checking (ERC), layout comparison (XOR), and parasitic extraction (PEX) in one engine, running production rule decks written in industry-standard rule deck syntax natively — no translation step. LVR is positioned as a pre-signoff iteration platform: whole-team access at a fraction of signoff seat cost, so verification runs on every save, not only at milestones.

5	230+	native	near-linear
engines: DRC · LVS · ERC · XOR · PEX	geometric checking primitives	industry-standard rule deck syntax	multicore scaling

Capabilities at a glance

Engine	Scope
DRC	full-chip and cell-level geometric checking: spacing, width, enclosure, extension, density (windowed and gradient), connectivity-aware and voltage-aware check classes; hierarchical execution; result caps honored as the deck states them
LVS	device extraction from layout, netlist reduction, topology comparison against CDL/SPICE, parameter checking (W/L/m), pin-to-net verification, mismatch diagnosis panes
ERC	net-rule and device-rule electrical checks on the extracted connectivity
XOR	hierarchical layout-to-layout comparison with per-layer difference reporting
PEX	resistance and capacitance extraction with coupling, SPEF and DSPF output for any industry static timing tool — including Ramtera PRE

Data and ecosystem

GDSII and OASIS layout input and output with hierarchical round-trip fidelity; CDL/SPICE and Verilog netlists; results browsable in LVR's own results viewer or pushed as native markers into major custom-IC layout environments; persistent violation waivers that survive layout edits and ECOs. Open process design kits — SKY130, IHP SG13G2, GF180MCU — are supported out of the box for evaluation and education.

Platform

Linux x86-64. Command-line batch for farms and continuous integration; GUI for interactive debug. Scales from a 4-core workstation to cloud fleets — Ramtera's reference full-chip run used 1,024 vCPU (512 physical cores) on a public cloud. Peak memory is user-tunable: it scales with the thread count times the working tile footprint, so the same design runs on small machines with fewer threads.

LICENSING — Licensing: node-locked license files (hostname + hardware address) standard; floating concurrent pools via industry-standard license-manager infrastructure for enterprise deployments. Prices are always quoted with their seat count.

Engagement

30-day supported evaluation on your designs, on your machines — layouts never leave your premises. 90-day paid pilot with success criteria agreed up front. Production licensing thereafter. See the Evaluation Process and Security

documents in this series.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.