RAMTERA

PRODUCT DOCUMENTATION · PHYSICAL VERIFICATION (LVR)

RAMTERA-LVR-IOF

Supported Input and Output Formats

The format reference for flow integration, with conformance evidence

August 2026 · Ramtera PRE engineering

LVR Supported Input and Output Formats

This document is the format reference for flow integration: what LVR reads, what it writes, and the conformance statements behind each. Detailed conformance evidence lives in the white paper series (WP-03 layout round-trip, WP-05 database units, WP-06 results interoperability, WP-07 netlist robustness, WP-10 deck coverage, WP-11 OASIS).

2	2	native	markers
layout formats, hierarchical round-trip	parasitic output formats	rule deck execution	into layout environments

Inputs

Format	Use	Notes
GDSII	layout in	full hierarchy: structures, references, arrays, text; exact database-unit handling with automatic rescaling across mismatched libraries
OASIS	layout in	modal-state reader validated against reference streams (WP-11)
Rule decks	checking	industry-standard rule deck syntax executed natively — production foundry decks run as shipped; preprocessor conditionals, includes, layer maps, groups
CDL / SPICE	LVS source	subcircuits, m-factors, parameters; robust continuation and comment handling (WP-07)
Verilog (structural)	netlist compare	gate-level netlists for digital LVS flows
Layer map files	I/O control	layer/datatype mapping for stream in and out

Outputs

Format	Use	Notes
Results database + reports	DRC/LVS/ERC/XOR	per-rule, per-cell violation data; ASCII summaries; browsable in the results viewer
SPEF	parasitics	IEEE 1481 output consumed by industry static timing tools; validated against Ramtera PRE's hand-verified SPEF reader (PRE series WP-15)
DSPF	parasitics	detailed standard parasitic format for analog flows
GDSII / OASIS	layout out	hierarchical write-back; round-trip fidelity gated by layout XOR in regression (WP-03)
Marker export	debug	violations as native markers in major custom-IC layout environments, with read-back for waiver assignment

Format	Use	Notes
Waiver database	signoff hygiene	persistent, edit-surviving waivers stored separately from results

HOW TO READ THIS TABLE — Conformance discipline: every format claim above is backed either by a published white paper with measured evidence or by the regression suite's round-trip gates. Where a format subset is partial, the subset is documented rather than implied whole.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.