RAMTERA

PRODUCT DOCUMENTATION · PHYSICAL IMPLEMENTATION (PRE)

RAMTERA-PRE-BM

Benchmark Methodology

Correctness by golden testcase, QoR with legality, exact distributed equality

August 2026 · Ramtera PRE engineering

PRE Benchmark Methodology

Implementation tools are measured on quality of results, correctness, and runtime — and each is easy to misreport. This document fixes PRE's method, applied to Ramtera's own published numbers first and to pilot measurements second.

3	golden	declared	exact
axes: correctness, QoR, runtime	hand-computed testcases for correctness	environment for every figure	acceptance bar for distributed timing

Correctness: golden testcases before correlation

Timing correctness is validated on designs small enough that every printed digit is re-derivable by hand — library interpolation, wire delay, required-time arithmetic (white paper WP-16). Physical engines validate by identity: filler area equals free span exactly; antenna ratios reproduce from the LEF numbers in closed form; stream-out is checked by an independent parser. Correlation against other tools is used for modeling comparisons, never as the correctness proof.

Quality of results

Rule	Why
HPWL, legality, and displacement reported together	wirelength without legality is fiction; the placement papers report all three (WP-20)
Engine and mode disclosed per number	PRE has two global placers; every figure names which ran
Unfavorable comparisons published	the 2,000-cell case where the simpler engine wins by 30% is in the published record — a methodology that only reports wins is marketing
Timing QoR on stated views	WNS/TNS quoted with the view, corner scaling, and clock that produced them

Runtime and scaling

Fixed design, fixed flow, declared environment, thread sweep with wall time and peak memory per point — the same protocol as LVR's. Distributed timing has a stricter bar than speed: the distributed result must equal the local result exactly, on a test constructed so corners produce distinct nonzero slacks (WP-21) — a test all-zero slacks cannot fake.

YOUR NUMBERS STAY YOURS — In pilots, this methodology runs on your blocks and the numbers are yours. Ramtera publishes nothing from customer engagements without written permission.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.