RAMTERA

PRODUCT DOCUMENTATION · PHYSICAL IMPLEMENTATION (PRE)

RAMTERA-PRE-DS

PRE Product Datasheet

Floorplan to GDSII on industry-standard command conventions — pre-signoff economics

August 2026 · Ramtera PRE engineering

PRE — Physical Implementation Environment

PRE is Ramtera's place-and-route platform: floorplanning, global and detailed placement, clock tree synthesis, global and detailed routing, multi-corner static timing with optimization, power intent (UPF), power-grid synthesis with IR analysis, and tapeout-shaped GDSII — behind a Tcl command surface built on industry-standard implementation-tool conventions, so existing flow scripts and operator skills transfer directly. PRE is positioned as a pre-signoff iteration environment: whole-team access at a fraction of signoff seat cost.

135	50,000	native	exact
Tcl commands, 12 flow stages	cells placed in the scale reference	SDC + UPF sourcing	distributed = local timing

Capabilities at a glance

Stage	Scope
Floorplan	die/core, rows, tracks, macros, halos, blockages, fences/regions, pin constraints, pad ring and bump planning (33 commands)
Placement	quadratic global placer with density spreading plus a nonlinear analytical engine from Ramtera's placement research; legalization; incremental refinement; one command surface
Clock tree	H-tree synthesis on real flop sinks, buffer sizing from a declared list, clock non-default routing rules
Routing	global routing over capacity-aware GCells; detailed routing with spacing checked in-loop — clean by construction
Timing	NLDM library timing with slew propagation, SPEF (IEEE 1481) parasitics, SDC path exceptions with the documented priority model, MMMC views, setup and hold optimization
Power	UPF subset natively sourced: domains, fences, isolation insertion, leakage recovery, power reporting; PG rings/stripes/rails with static IR and current-density checks
Signoff prep	filler/tap/end-cap insertion with exact-area validation, antenna check and repair, hierarchical GDSII stream-out

Evidence, not adjectives

The PRE white paper series (WP-13 through WP-22) publishes the validation behind this datasheet: SDC exception semantics reproduced against the documentation's own examples, SPEF delays hand-verified to 0.1 ps, GDSII checked by an independent record walker, antenna arithmetic in closed form, placement measured to 50,000 cells, and multi-host timing proven exactly equal to local analysis.

Platform and ecosystem

Linux x86-64; batch Tcl for farms and a Qt-based GUI for interactive work. Reads LEF/DEF/Verilog/liberty/SDC/UPF/SPEF; writes DEF, GDSII, and reports. Pairs with Ramtera LVR: LVR's parasitic extraction feeds PRE's timing through a validated SPEF contract — extraction and implementation from one vendor, verified against each other.

COMMERCIAL — Licensing and engagement match LVR: node-locked license files standard, floating pools for enterprises, 30-day evaluation, 90-day paid pilot, prices always quoted with seat counts.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.