RAMTERA

PRODUCT DOCUMENTATION · PHYSICAL IMPLEMENTATION (PRE)

RAMTERA-PRE-IOF

Supported Input and Output Formats

LEF/DEF/Verilog/liberty/SDC/UPF/SPEF in — DEF/GDSII/reports out

August 2026 · Ramtera PRE engineering

PRE Supported Input and Output Formats

The format reference for flow integration. Conformance evidence lives in the white paper series: SPEF in WP-15, GDSII in WP-17, SDC exception semantics in WP-14.

7	4	native	validated
input formats	output formats	SDC and UPF are sourced, not translated	against published golden testcases

Inputs

Format	Use	Notes
LEF	technology + macros	layers, sites, macro pins and obstructions, antenna properties (gate/diffusion areas, layer ratios)
DEF	design in	die, rows, tracks, components, pins, nets, placement status (FIXED honored throughout)
Verilog	netlist in	structural gate-level
Liberty	timing libraries	NLDM delay and transition tables, pin capacitances, leakage; multiple libraries per library set for MMMC
SDC	constraints	sourced natively on the interpreter — clocks, IO delays, derates, and the full path-exception set with documented priorities
UPF	power intent	sourced natively: domains, supplies, isolation strategies
SPEF	parasitics	IEEE 1481 subset: units, name maps, corner triplets with field selection, RC networks with coupling, multi-file hierarchical stitching, per-corner scaling

Outputs

Format	Use	Notes
DEF	snapshot out	placement and routing state for downstream tools
GDSII	tapeout-shaped stream	hierarchical: per-cell structures, per-instance references, pin labels, wires; layer map file; byte-stable across thread counts; validated by an independent record walker
Timing reports	analysis	per-hop path reports, per-view MMMC tables, exception application tables
Result line format	distributed collection	single-line machine-parseable STA results used by multi-host analysis

LVR INTEROP — The SPEF contract is shared with Ramtera LVR's extraction output and validated in both directions with hand-computable golden testcases — the basis of the single-vendor extraction-to-timing story.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

Contact

Web	www.ramtera.com
Inquiries	sameer@ramtera.com
Engineering	Bangalore, Karnataka, India

This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.