



RAMTERA

TECHNICAL WHITE PAPER SERIES · PHYSICAL IMPLEMENTATION (PRE)

RAMTERA-WP14

Faithful SDC Path-Exception Semantics

The documented priority model, implemented and validated against its own examples

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Faithful SDC Path-Exception Semantics: Implementing the Documented Priority Model

Timing exceptions — false paths, multicycle paths, maximum and minimum delay constraints — are where static timing tools quietly disagree. The industry reference publishes an explicit priority table for overlapping exceptions; PRE implements that table as written and validates the implementation against the reference documentation's own worked examples. This paper states the semantics PRE guarantees and shows the validation results.

8/8 documented example pairs reproduced	6 exception commands	2 check types (setup, hold)	exact hold-shift arithmetic verified
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The priority model

When one path matches several exceptions, resolution follows: false path over max/min delay over multicycle; within a class, an exception specifying more of -from/-through/-to wins; then -from outranks -to outranks -through; pin-based selectors outrank clock-based; ties resolve to the most constraining adjustment; and an exception with identical selectors overwrites its predecessor.

Validation against the documentation's own examples

Scenario	Expected	PRE result
false path (-from A -through B -to C) vs multicycle (-from A)	false wins on the ABC path; multicycle applies elsewhere	match
multicycle -from A 3 vs -to C 2	3 applies (-from over -to)	match
multicycle -through A -to B 3 vs -to B 2	3 applies (more selectors)	match
same selectors, second command	overwrite (later wins)	match
max_delay vs multicycle on same path	max_delay class wins	match
min_delay under hold analysis	applies to hold only	match
setup multicycle N, no hold multicycle	hold check moves to (N-1) cycles	match — required time exact
pin selector vs clock selector	pin-based outranks	match

End-to-end arithmetic

On a reference design with a 0.8 ns clock: a 0.30 ns maximum-delay constraint to an output port produced a required time of exactly 0.2000 ns (value minus the 0.10 ns external delay) and a slack of -0.0404 ns; declaring the input-to-register path false removed exactly that endpoint from analysis, with the report annotating the dropped count; a setup multicycle of 3 moved the hold-check required time to exactly $(3-1) \times 0.8 + 0.03 = 1.6300$ ns. Every number is closed-form checkable from the constraint values.

DIAGNOSTIC — An exception that matched no endpoint in the last analysis is reportable as ignored — the same diagnostic the reference documentation describes — so constraint-file rot is visible instead of silent.

```
set_max_delay 0.30 -to [get_ports out1]
set_false_path -from [get_ports inp1] -to F1/D
set_multicycle_path 2 -setup -from [get_clocks clk] -to [get_ports out1]
report_path_exceptions
  1 applied  set_max_delay 0.3 -setup -to {out1}
  2 applied  set_false_path -from {inp1} -to {F1/D}
  3 ignored  set_multicycle_path 2 -setup ...    ;# outranked, as documented
```

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.