RAMTERA

TECHNICAL WHITE PAPER SERIES · PHYSICAL IMPLEMENTATION (PRE)

RAMTERA-WP15

SPEF Conformance and Hand-Verified Delay Accuracy

IEEE 1481 parasitics driving RC-tree timing, checkable to 0.1 ps

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Standard Parasitic Exchange: SPEF Conformance and Hand-Verified Delay Accuracy

Post-route timing is only as good as the parasitics feeding it. PRE reads IEEE 1481 SPEF — units, name maps, corner triplets, hierarchical multi-file stitching — and drives its static timing from true per-net RC trees. This paper documents the supported subset and a validation method any customer can repeat: every delay figure below is checkable by hand from the SPEF text.

IEEE 1481 SPEF subset	**0.1 ps** agreement with hand computation	**3** corner-triplet field selection	**mixed** annotated + unannotated nets in one graph

Supported constructs

Construct	Handling
*T_UNIT / *C_UNIT / *R_UNIT	honored, including FF and KOHM multipliers
*DIVIDER / *DELIMITER	any single character; normalized internally
*NAME_MAP	*NNN and *NNN:pin references resolved
*D_NET / *CONN / *CAP / *RES	full RC network per net; grounded and coupling capacitors
corner triplets a:b:c	field selectable per read (-spef_field), default first
multiple files	hierarchical stitching: later files override same-name nets
scale factors	per-corner capacitance and resistance scaling applied as read (-scaleRC)

Hand-verifiable validation

A published two-sink RC tree (250 Ω + 250 Ω branches, known node capacitances) must produce Elmore delays of exactly 3.000 ps and 3.500 ps and a driver load of 0.020 pF. PRE reproduces all three to the displayed precision. Selecting corner field 2, where one resistor's triplet carries 999 Ω, moves the first sink to exactly 6.995 ps. Applying 1.4× cap and resistance scaling moves it to exactly 5.152 ps with a 0.0252 pF load. On a routed reference design, every arrival increment along the reported worst path matches the closed-form value: the register launch at 0.0675 ns, then +5.5 ps, +64 ps, and +9.6 ps of wire delay hop by hop.

ROBUSTNESS — Nets absent from the SPEF fall back to the geometric wire model inside the same timing graph, and the analysis banner reports the annotation ratio (for example, SPEF 4/6 nets) — partial annotation is visible, never silent.

Why this matters for extraction flows

Because the reader's contract is precise and published, any extractor — including Ramtera's LVR parasitic extraction — can be validated against PRE timing with a golden testcase whose answers are computable by hand. The conformance surface in this paper is that contract.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.