



RAMTERA

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RAMTERA-WP16

Hand-Computed Golden Testcases for Timing Engines

Every printed digit re-derived independently — correctness, not just correlation

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Hand-Computed Golden Testcases: A Verification Methodology for Static Timing Engines

Timing engines are usually validated by correlation against another tool — which proves agreement, not correctness. PRE's timing engine is additionally validated against testcases small enough that every number in the report is derivable with a calculator: library table lookups, wire delays, required times, and slacks. This paper describes the methodology and publishes a worked example.

100% of reported hops closed-form checked	2 check types validated (setup, hold)	4 constraint mechanisms exercised	0 unexplained digits in the report
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The method

A testcase is built from a two-cell library with single-row delay tables, a four-instance netlist with one register, and parasitics simple enough to evaluate manually. For each reported path, three classes of number are re-derived independently: (1) cell arc delays by interpolating the library table at the exact load the engine reports; (2) wire delays from the RC network by the standard first-moment formula; (3) required times from the clock period, external delays, margins, and any exception arithmetic. The engine passes only if every digit printed is reproduced.

Worked example (0.8 ns clock)

Report line	Independent derivation	Match
register launch 0.0675 ns	table row 0.065@0.01pF..0.090@0.05pF interpolated at 0.014 pF	yes
+0.0055 ns wire	$250\Omega \cdot 0.014\text{pF} + 250\Omega \cdot 0.008\text{pF} = 5.5\text{ ps}$	yes
+0.0550 ns cell	table at 0.042 pF load	yes
+0.0640 ns wire	$1000\Omega \cdot 0.042\text{pF} + 1000\Omega \cdot 0.022\text{pF}$	yes
required 0.7000 ns	period – 0.10 ns output delay	yes
hold required 1.6300 ns	$(3-1) \cdot 0.8 + 0.03$ (multicycle shift)	yes

METHODOLOGY — The same discipline applies to physical engines: filler insertion is validated by exact free-area accounting, and antenna checking by closed-form charge-ratio arithmetic. When a report digit cannot be re-derived, that is a bug by definition.

What correlation cannot give you

Correlation against a reference tool inherits the reference's approximations and bugs, and offers no explanation when the two disagree. Golden hand computation localizes any disagreement to a specific arc, wire, or required-time term. Ramtera uses both: golden testcases prove the arithmetic; correlation on larger designs proves the modeling.

About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

Contact

Web	www.ramtera.com
Inquiries	sameer@ramtera.com
Engineering	Bangalore, Karnataka, India

This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.