RAMTERA

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RAMTERA-WP18

Process Antenna Verification and Repair

Closed-form charge-ratio checking with layer-jump and diode repair

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Process Antenna Verification with Closed-Form Arithmetic and Two-Mode Repair

Plasma-induced gate damage is checked from the routed geometry against the antenna properties the technology LEF declares. PRE's checker follows the LEF semantics — gate and diffusion areas on pins, area ratios on layers — with a cumulative charge-ratio model whose every violation is checkable by hand, and repairs violations by layer reassignment or protection-diode insertion. This paper shows the model and a fully worked repair.

closed-form every ratio hand-checkable	**2** repair modes (layer jump, diode)	**0** violations after repair on the reference run	**per-net** geometry attribution

The model, stated exactly

For each net and each routing layer k, the accumulated conductor area on layers up to k is compared against ratio(k)·gateArea + diffRatio(k)·diffArea, where the ratios come from the LEF layer statements and the areas from the LEF pin statements summed over the net's connections. A net without gate area cannot violate; declared diffusion raises the budget linearly. The report prints area, gate, diffusion, the resulting charge ratio, and the limit for every row.

Worked violation

On the reference design, a clock net accumulates 14.76 µm² of conductor by the top layer against a 0.03 µm² gate: the printed ratio is exactly 492.00 = 14.76 / 0.03, against a limit of 400 — flagged. Nets carrying 0.02 µm² of driver diffusion show a limit of exactly 480 = 400 + 200·0.02/0.05 — every limit reproduces from the LEF numbers.

Two-mode repair, exercised on both paths

Situation	Action	Reference-run result
violation below the top layer, tighter 250 limit	largest offending shape reassigned one layer up, re-verified per step	11 reassignments removing exactly the 1.06 µm² the layer budget required (0.10 µm² per step)
violation on the top layer (nowhere to jump)	protection diode placed beside the endangered gate and attached to the net; its declared diffusion raises the budget	one diode at the register, net clean
after both	full re-verify	0 violations, all nets

STATED BOUNDARY — Layer reassignment here is a post-route engineering change: spacing on the destination layer is not re-checked by the repair itself. Re-running the router restores clean-by-construction spacing. The paper states this boundary because a repair tool that hides its boundaries is a liability.

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verifyProcessAntenna -detailed -report ant.rpt
  net nclk  M4  cumArea 14.7600  gate 0.0300  PAE 492.00  limit 400  *VIOLATED*
fixAntenna -layerJump -diodeCell ANTDIODE
  11 layer jump(s), 1 diode(s) -> 0 violation(s) remain
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About Ramtera

Ramtera Inc. (Delaware, USA), with R&D at Ramtera Design Automation India Pvt Ltd (Bangalore), builds electronic design automation software for physical verification and physical implementation. LVR is Ramtera's physical verification engine (DRC, LVS, ERC, XOR, parasitic extraction); PRE is Ramtera's physical implementation environment (floorplanning, placement, clock tree synthesis, routing, timing analysis and optimization), built on industry-standard command conventions so existing flow scripts and operator skills transfer directly. The company holds granted patents and registered copyrights covering its engines.

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This document reports measurements from Ramtera's engineering environment (Ubuntu 24.04, GCC 13.3, Tcl 8.6) unless stated otherwise. Product behavior and figures are subject to change; no compatibility, certification, or endorsement by any third party is stated or implied.